


Snoopy Coherence Protocols

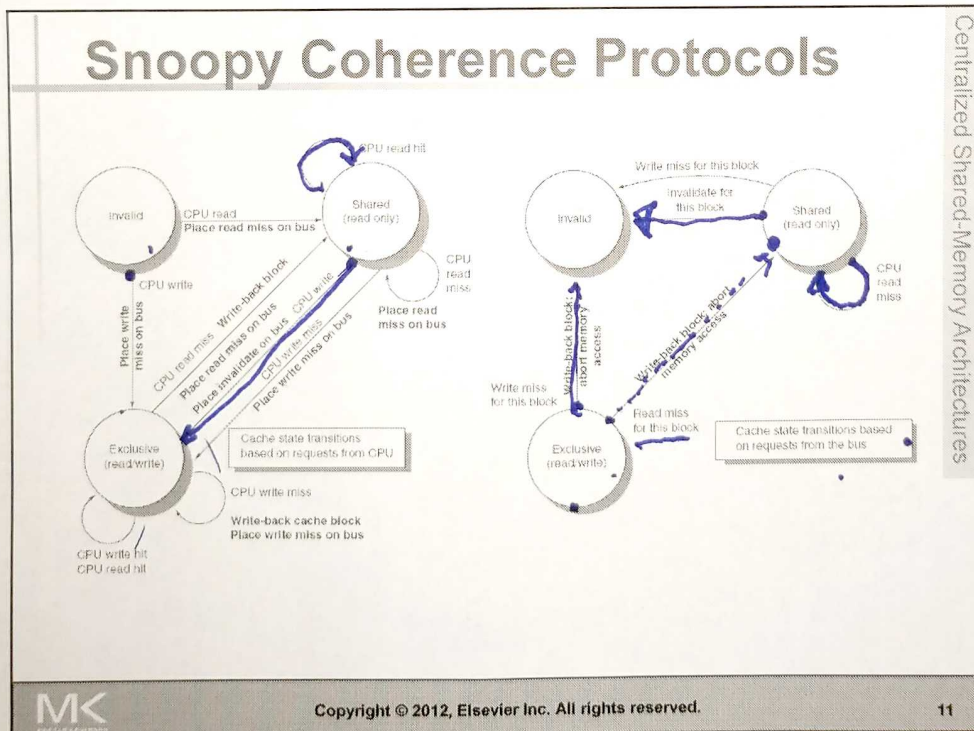
Request	Source	State of addressed cache block	Type of cache action	Function and explanation
Read hit	Processor	Shared or modified	Normal hit	Read data in local cache.
Read miss	Processor	Invalid	Normal miss	Place read miss on bus.
Read miss	Processor	Shared	Replacement	Address conflict miss: place read miss on bus.
Read miss	Processor	Modified	Replacement	Address conflict miss: write-back block, then place read miss on bus.
Write hit	Processor	Modified	Normal hit	Write data in local cache.
Write hit	Processor	Shared	Coherence	Place invalidate on bus. These operations are often called upgrade or <i>ownership</i> misses, since they do not fetch the data but only change the state.
Write miss	Processor	Invalid	Normal miss	Place write miss on bus.
Write miss	Processor	Shared	Replacement	Address conflict miss: place write miss on bus.
Write miss	Processor	Modified	Replacement	Address conflict miss: write-back block, then place write miss on bus.
Read miss	Bus	Shared	No action	Allow shared cache or memory to service read miss.
Read miss	Bus	Modified	Coherence	Attempt to share data: place cache block on bus and change state to shared.
Invalidate	Bus	Shared	Coherence	Attempt to write shared block: invalidate the block.
Write miss	Bus	Shared	Coherence	Attempt to write shared block: invalidate the cache block.
Write miss	Bus	Modified	Coherence	Attempt to write block that is exclusive elsewhere; write-back the cache block and make its state invalid in the local cache.



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Centralized Shared-Memory Architectures

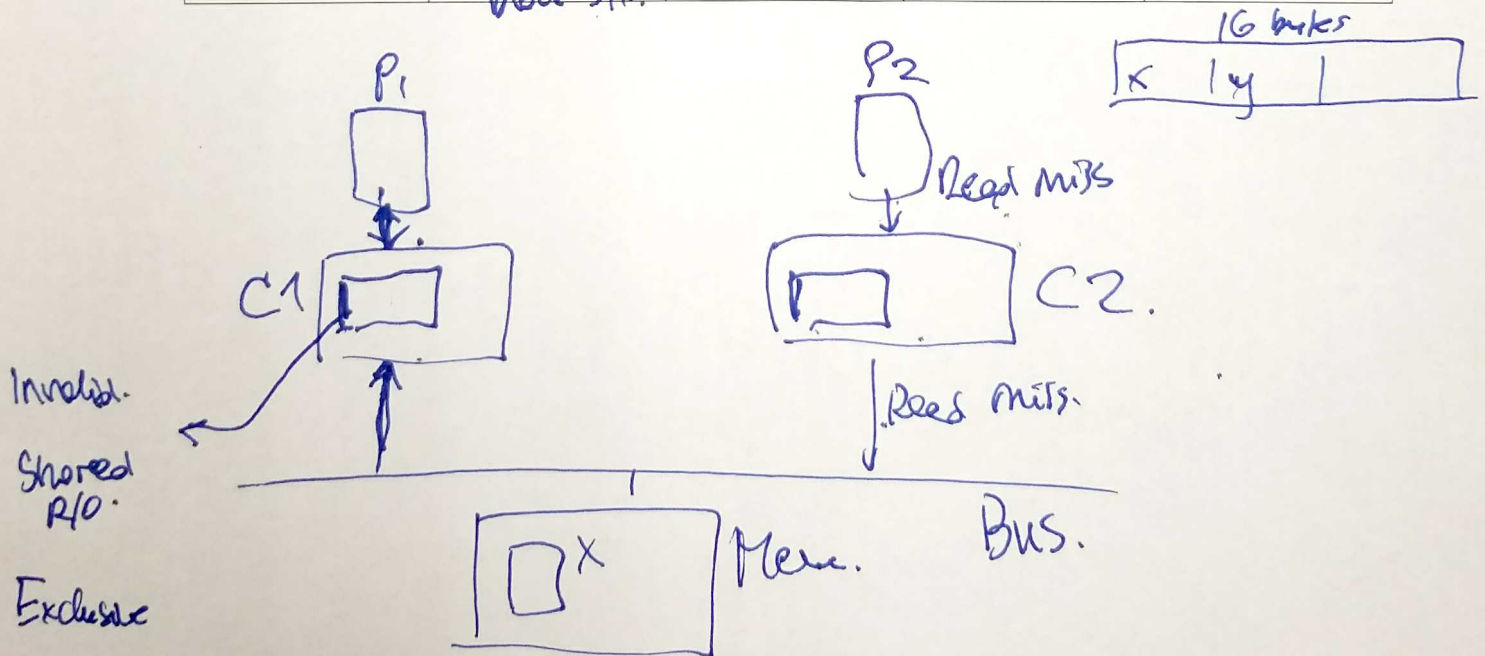


Centralized Shared-Memory Architectures

Problem 2 (25 points)

Consider an SMP system with two processors A and B using the MSI snoop cache coherence protocol. Assume we have memory location X addressed by the two processors. In the following table, you see the series of memory accesses by the two processors. Fill in the remainder of the table similarly to the first three rows.

Processor activity	Bus activity	Content of Proc A's cache	Contents of Proc B's cache	Contents of mem location X
A writes X=2	Write miss.	Exclusive x=2	Invalid.	x=0.
B reads X	Read miss B, x. Write back A	Shared x=2	Shared x=2.	x=2
A reads x. A writes X=3	Invalidate.	Exclusive x=3	Invalid.	
B reads X	Read miss B, x Write back A	Shared x=3	Shared x=3	x=3
B writes X = 5	Invalidate	Invalid.	Exclusive x=5	x=3
A writes X=1 y=1	Write miss. Write back block B, X.	Exclusive x=1 y=1	Invalid.	x=5. y=0



		A	B	Memory
-	-	Invalid	Invalid	$x = 0$
A read x	Read miss A, x	Shared $x = 0$	Invalid	$x = 0$
B read x	Read miss B, x	Shared $x = 0$	Shared $x = 0$	$x = 0$