Problem NUMA system directory based cache coherence protocol (Given HW2, Fall 2016)

Let us consider a NUMA system using directory based cache coherence. Let us assume that there are two processors:

- Proc A, which has memory locations M=#A000 - #AFFF, cache A and directory A
- Proc B, which has memory locations M=#B000 - #AFFF, cache B and directory B

Assume all memory locations are initialized to 0. The events creates by a memory access can be traced as follows:

1. **Proc A reads memory location #B001**

Messages:

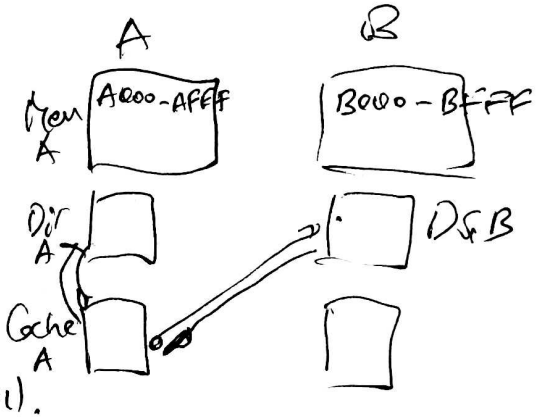
Message "Read Miss" from Cache A to Directory B: (A, #B001)
Message "Data value reply" from Directory B to Cache A: value = 0

Results

Memory B: value at #B001 = 0
Directory B: State of #B001 = Shared, sharers {A}
Cache A: Value of #B001 = 0

Trace the following events:

2. Proc A reads memory location #A001
3. Proc B reads memory location #B001
4. Proc A writes memory location #B001 with 2
5. Proc A reads memory location #A001
6. Proc B writes memory location #B001 with 3



(2) Msg ReadMiss CacheA to DirA (A, #A001).
Msg Data value reply DirA → CacheA.

Results
Mem A = #A001 = 0
Dir A State of #A001 = Shared, Sharers = {A}.
Cache A = Value of #A001 = 0.

(3) Proc B reads #B001.
= Directory B State of #B001 = Shared, Sharers = {A, B}.

(4) Proc A writes #B001 with 2.
Cache A sends Dir B write miss. A, #B001.
Dir B sends Cache B invalidate.

Results:
A writes in Cache A #B001 = 2. ✓
Mem in B #B001 = 0. ✓
Cache B of #B001 is invalid.
Dir B #B001 is Modified "owner = A".