COP 5106 - Fall 2017 - Homework 2

Due: November 13, 2017

Consider the following C++ program fragment:

- a) Write a MIPS assembly program that corresponds to this program fragment.
- b) Identify RAW, WAW and WAR hazards in the resulting code
- c) Assuming that you have instruction latencies like in the following table, insert stall states into the resulting code.

Instruction producing result	Instruction using result	Latency in clock cycles
FP ALU op	Another FP ALU op	3
FP ALU op	Store double	2
Load double	FP ALU op	1
Load double	Store double	0

- d) Unroll the resulting assembly program 2 times in software.
- e) Transform the program by pipeline scheduling such that the number of stalls is minimized.
- f) Discuss the performance of the program. What is the bottleneck? Can you think of other ways in which this code fragment can be optimized?