Cyber Security & Privacy Cluster

"Designing Secure Multicore Systems from Untrusted Components"

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Abstract - The current trend in system-on-chip (SoC) design is system-level integration of heterogeneous technologies consisting of a large number of processing elements such as programmable RISC cores, memories, DSPs, and accelerator function units/ASIC. These processing elements may come from different providers, and application executable code may have varying levels of trust. Some of the pressing, security-related, architecture design questions are: (1) how to implement multi-level user-defined security; (2) how to optimally and securely share resources and data among processing elements; (3) how to use reconfiguration for the purpose of obfuscation to attackers. In this talk, I will present a secure multicore architecture that integrates multiple processing elements (which may include secure and non-secure cores) into the same chip design, while (i) maintaining individual security, (ii) preventing data leakage and corruption, and (iii) enforcing secure resource sharing among mutually distrusting processing elements or applications.

About Dr. Kinsy - Michel A. Kinsy is an Assistant Professor in the Department of Electrical and Computer Engineering at Boston University (BU), where he directs the Adaptive and Secure Computing Systems (ASCS) Laboratory. He focuses his research on computer architecture, hardware-level security, and neural network accelerator designs. Dr. Kinsy is an MIT Presidential Fellow, the 2018 IEEE MWSCAS Myril B. Reed Best Paper Award Recipient, DFT'17 Best Paper Award Finalist, and FPL'11 Tools and Open-Source Community Service Award Recipient. Dr. Kinsy earned his PhD in Electrical Engineering and Computer Science in 2013 from the Massachusetts Institute of Technology. His doctoral work in algorithms to emulate and control large-scale power systems at the microsecond resolution inspired further research by the MIT spin-off Typhoon HIL, Inc. Before joining the BU faculty, Dr. Kinsy was an assistant professor in the Department of Computer and Information Systems at the University of Oregon, where he directed the Computer Architecture and Embedded Systems (CAES) Laboratory. From 2013 to 2014, he was a Member of the Technical Staff at the MIT Lincoln Laboratory.

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Time:
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Location:
Research 1, Rm 101

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