UNIVERSITY OF CENTRAL FLORIDA
DEPARTMENT OF COMPUTER SCIENCE
& FACULTY CLUSTER INITIATIVE

Cyber Security & Privacy Cluster

"Heterogeneous Systems in the Era of Exascale and Beyond"

Jagadish Kotra, Ph.D.

AMD Research

Date:
Thursday, 2/27/20

Time:
11:00am-12:30pm

Location:
Research 1, Rm 101

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Abstract - Heterogeneous systems are ubiquitous and are deployed in a wide variety of devices ranging from low-end mobile systems to high-end datacenters and supercomputers. This heterogeneity is prevalent in both compute (CPUs/GPUs and FPGAs) and memory (HBM/Off-chip DDR-x) resources. However, programming these systems pose several challenges to domain-specific researchers developing HPC applications as they must now worry about the nuances involved in: (1) orchestrating the data movement, and, (2) managing data placement (memory over-subscription) in accelerators. To address this problem, exascale systems that employ accelerators (GPUs) as true peers to general purpose CPUs have been proposed.

In this talk, I will present my on-going and previous research that optimizes such programmer-friendly heterogeneous systems. Specifically, I will present my on-going work on dynamically reconfigurable GPU architecture that alleviates the virtual memory bottlenecks by repurposing the on-chip hardware structures opportunistically. On the memory front, I will present a hardware-software co-designed heterogeneous memory system that reconfigures dynamically based on the workloads executing on the system. If time permits, I will briefly cover my other research projects before presenting my near and long-term research directions.

About the candidate - Jagadish Kotra is a researcher at AMD Research (in Austin), where he is currently working on optimizing AMD's Exascale Heterogeneous Processor (EHP) node architecture. This research is aimed at building nation's first exascale supercomputer and is funded by Department of Energy (DoE) as part of the Path Forward project. He obtained his Ph.D from The Pennsylvania State University in 2017. At Penn State, his thesis proposed solutions that targeted bridging the performance gap between the multi/many-core processors and memory. To that end, he proposed hardware-only, software-only and hardware-software co-design based solutions that spanned multiple layers of the system stack. Jagadish's work appeared in several top-tier research venues and he has around 10 patents that are either granted or under filing in US Patent Office (USPTO) from his stints at various industry labs.