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Accelerating the discontinuous Galerkin method for seismic wave propagation simulations using multiple GPUs with CUDA and MPI

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8 **Abstract** We have successfully ported an arbitrary high-9 order discontinuous Galerkin method for solving the three-10 dimensional isotropic elastic wave equation on unstruc-11 tured tetrahedral meshes to multiple GPU using CUDA and 12 MPI and obtained a speedup factor of about 28.3 for the 13 single-precision version of our codes and a speedup factor 14 of about 14.9 for the double-precision version. The GPU 15 used in the comparisons is NVIDIA Tesla C2070 Fermi, 16 and the CPU used is Intel Xeon W5660. To effectively 17 overlap inter-process communication with computation, we 18 separate the elements on each subdomain into inner and 19 outer elements and complete the computation on outer 20 elements and fill the MPI buffer first. While the MPI 21 messages travel across the network, the GPU performs 22 computation on inner elements, and all other calculations 23 that do not use information of outer elements from neigh-24 boring subdomains. A significant portion of the speedup 25 also comes from a customized matrix-matrix multiplica-26 tion kernel, which is used extensively throughout our 27 program. Preliminary performance analysis on our parallel 28 GPU codes shows favorable strong and weak scalabilities.

30 Keywords Seismic wave propagation · Discontinuous
 31 Galerkin · GPU

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1 Introduction

Computer simulations of seismic wavefields have been 33 playing an important role in seismology in the past few 34 decades. However, the accurate and computationally effi-35 cient numerical solution of the three-dimensional elastic 36 seismic wave equation is still a very challenging task, 37 especially when the material properties are complex, and 38 39 the modeling geometry, such as surface topography and subsurface fault structures, is irregular. In the past, several 40 numerical schemes have been developed to solve the 41 elastic seismic wave equation. The finite-difference (FD) 42 43 method was introduced to simulate SH and P-SV waves on regular, staggered-grid, two-dimensional meshes in Ma-44 dariaga (1976) and Virieux (1984, 1986). The FD method 45 was later extended to three spatial dimensions and to 46 47 account for anisotropic, visco-elastic material properties (e.g., Mora 1989; Igel et al. 1995; Tessmer 1995; Graves 48 1996; Moczo et al. 2002). The spatial accuracy of the FD 49 50 method is mainly controlled by the number of grid points required to accurately sample the wavelength. The pseudo-51 spectral (PS) method with Chebychev or Legendre poly-52 53 nomials (e.g., Carcione 1994; Tessmer and Kosloff 1994; Igel 1999) partially overcomes some limitations of the FD 54 method and allows for highly accurate computations of 55 spatial derivatives. However, due to the global character of 56 its derivative operators, it is relatively cumbersome to 57 58 account for irregular modeling geometries, and efficient 59 and scalable parallelization on distributed-memory computer clusters is not as straightforward as in the FD method. 60 Another possibility is to consider the weak (i.e., varia-61 tional) form of the seismic wave equation. The finite-ele-62 ment (FE) method (e.g., Lysmer and Drake 1972; Bao et al. 63 1998) and the spectral-element (SE) method (e.g., Ko-64 matitsch and Vilotte 1998; Komatitsch and Tromp 1999, 65



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66 2002) are based on the weak form. An important advantage of such methods is that the free-surface boundary condition 67 68 is naturally accounted for even when the surface topogra-69 phy is highly irregular. And in the SE method, high-order 70 polynomials (e.g., Lagrange polynomials defined on 71 Gauss-Lobatto-Legendre points) are used for approxima-72 tion, which provide a significant improvement in spatial 73 accuracy and computational efficiency.

74 The arbitrary high-order discontinuous Galerkin (ADER-75 DG) method on unstructured meshes was introduced to 76 solve two-dimensional isotropic elastic seismic wave 77 equation in Käser and Dumbser (2006). It was later exten-78 ded to three-dimensional isotropic elastic case in Dumbser 79 and Käser (2006) and to account for viscoelastic attenuation 80 (Käser et al. 2007), anisotropy (la Puente De et al. 2007) and 81 poroelasticity (la Puente et al. 2008). The p-adaptivity (i.e., 82 the polynomial degrees of the spatial basis functions can 83 vary from element to element) and locally varying time 84 steps were addressed in Dumbser et al. (2007). Unlike 85 conventional numerical schemes, which usually adopt a 86 relatively low-order time-stepping method such as the 87 Newmark scheme (Hughes 1987) and the 4th-order Runge-88 Kutta scheme (e.g., Igel 1999), the ADER-DG method 89 achieves high-order accuracy in both space and time by 90 using the arbitrary high-order derivatives (ADER), which 91 was originally introduced in Toro (1999) in the finite-vol-92 ume framework. The ADER scheme performs high-order 93 explicit time integration in a single step without any intermediate stages. In three dimensions, the ADER-DG scheme 94 95 achieves high-order accuracy on unstructured tetrahedral 96 meshes, which allows for automated mesh generation even 97 when the modeling geometry is highly complex. Further-98 more, a majority of the operators in the ADER-DG method 99 are applied in an element-local way, with weak element-to-100 element coupling based on numerical flux functions, which 101 result in strong locality in memory access patterns. And the 102 high-order nature of this method lets it require fewer data 103 points, therefore, fewer memory fetches, in exchange for 104 higher arithmetic intensity. These characteristics of the 105 ADER-DG method make it well suited to run on massively 106 parallel graphic processing units (GPUs).

107 In the past four decades, the development in the com-108 puting chip industry has been roughly following the Moore's 109 law. Many of the performance improvements were due to 110 increased clock speeds and sophisticated instruction sched-111 uling in a single core. As the transistor density keeps increasing, the industry is now facing a number of engi-112 113 neering difficulties with using a large number of transistors 114 efficiently in individual cores (e.g., power consumption, 115 power dissipation). The effect is that clock speeds are 116 staying relatively constant, and core architecture is expected 117 to become simpler, if changes much at all. As a consequence, 118 when we consider future platforms for high-performance

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scientific computing, there are some inevitable trends, for 119 120 instance, the increase in the number of cores in generalpurpose CPUs and the adoption of many-core accelerators 121 (e.g., Field Programmable Gate Array, Graphic Processing 122 Unit, Cell Broadband Engine) due to their smaller footprints 123 124 and lower power consumptions than general-purpose CPUs. The users who want to once again experience substantial 125 performance improvements as before need to learn how to 126 exploit multiple/many cores. The GPU is becoming an 127 128 attractive co-processor for general-purpose scientific computing due to its high arithmetic computation power, large 129 memory bandwidth, and relatively lower costs and power 130 consumptions per FLOP, when compared with a typical 131 CPU. A typical GPU (e.g., NVIDIA GeForce 9800) can 132 reach a peak processing rate of 700 GFLOPS (1 133 $GFLOPS = 10^9$ floating-point-operations per second) and a 134 peak memory bandwidth of 70 GB/s. Unlike in a conven-135 tional CPU, in a GPU, many more transistors are dedicated 136 for data processing rather than data caching or flow control, 137 which makes GPUs particularly well suited to address 138 problems that can be expressed as data-parallel computa-139 tions. Recent efforts by GPU vendors, in particular, NVI-140 DIA's CUDA (Compute Unified Device Architecture) 141 programming model, the OpenCL (Open Computing Lan-142 guage) framework, and the OpenACC compiler directives 143 and APIs, have significantly increased the programmability 144 of commodity GPUs. Using these tools, a programmer can 145 146 directly issue and manage data-parallel computations on GPUs using high-level instructions without the need to map 147 them into a set of graphic-processing instructions. 148

149 With the rapid development of the GPU programming tools, various numerical algorithms have been successfully 150 ported to GPUs, and GPU-CPU hybrid computing plat-151 152 forms and substantial speedups, compared with pure-CPU implementations, have been achieved for applications in 153 different disciplines. The discontinuous Galerkin (DG) 154 method for solving the 3D Maxwell's equations, which are 155 linear, hyperbolic systems of conservation laws similar to 156 157 the seismic wave equation, has been successfully mapped to GPU using NVIDIA's CUDA framework and achieved 158 more than an order of magnitude speed-up compared with 159 the same implementation on a single current-generation 160 CPU (Klöckner et al. 2009). The GPU implementation was 161 done on a single NVIDIA GTX 280, which costs around 162 \$400. A significant portion of the speed-up came from the 163 high-order nature of the DG method. In the area of 164 acoustic/elastic seismic wave propagation simulations, the 165 finite-difference and the spectral-element methods have 166 been successfully implemented on CPU-GPU hybrid 167 clusters using the CUDA programming model (e.g., Abd-168 elkhalek et al. 2009; Komatitsch et al. 2009; Komatitsch 169 et al. 2010; Michéa and Komatitsch 2010; Okamoto et al. 170 171 2010; Wang et al. 2010). The speedup obtained varies from

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172around $20 \times$ to around $60 \times$ depending on several factors,173e.g., whether a particular calculation is amenable to GPU174acceleration, how well the reference CPU code is opti-175mized, the particular CPU and GPU architectures used in176the comparisons, and the specific compilers, as well as the177compiler options, used for generating the binary codes.

178 In Mu et al. (2013), we successfully ported the ADER-DG 179 method for solving three-dimensional elastic seismic wave 180 equation to a single NVIDIA Tesla C2075 GPU using 181 CUDA and obtained a speedup factor of about 24 when 182 compared with the serial CPU code running on one Intel 183 Xeon W5880 core. In this article, we explore the potential of 184 accelerating the ADER-DG method using multiple NVIDIA 185 Fermi GPUs with CUDA and the Message-Passing Interface 186 (MPI). Our reference CPU code is a community code named "SeisSol." The "SeisSol" code was written in Fortran 90 187 188 and parallelized using the Message-Passing Interface (MPI). It implements the ADER-DG method for solving the three-189 190 dimensional seismic wave equation in different types of 191 material properties (e.g., elastic, visco-elastic, anisotropic, 192 poroelastic). It has been optimized for different types of 193 CPU architectures and applied extensively in seismic wave 194 propagation simulations related to earthquake ground-195 motion prediction, volcano seismology, seismic exploration, 196 and dynamic earthquake rupture simulations. For a complete 197 list of the references of its applications, please refer to the 198 "SeisSol Working Group" website or la Puente et al. (2009). 199 The lessons learned in our implementation and optimization 200 experiments may also shed some light on how to port this 201 type of algorithms to GPUs more effectively using other 202 types of GPU programming tools such as OpenCL and 203 OpenACC.

204 2 CUDA programming model

205 For readers who are not familiar with CUDA or GPU 206 programming, we give a very brief introduction about the 207 programming model in this section. The CUDA software 208 stack is composed of several layers, including a hardware 209 driver, an application programming interface (API), and its 210 runtime environment. There are also two high-level, 211 extensively optimized CUDA mathematical libraries, the 212 fast Fourier transform library (CUFFT) and the basic linear 213 algebra subprograms (CUBLAS), which are distributed 214 together with the software stack. The CUDA API com-215 prises an extension to the C programming language for a 216 minimum learning curve. The complete CUDA program-217 ming toolkit is distributed free of charge and is regularly 218 maintained and updated by NVIDIA.

A CUDA program is essentially a C program with multiple subroutines (i.e., functions). Some of the subroutines
may run on the "host" (i.e., the CPU), and others may run on

the "device" (the GPU). The subroutines that run on the 222 device are called CUDA "kernels." A CUDA kernel is 223 typically executed on a very large number of threads to 224 exploit data parallelism, which is essentially a type of single-225 instruction-multiple-data (SIMD) calculation. Unlike on 226 227 CPUs where thread generation and scheduling usually take thousands of clock cycles, GPU threads are extremely "light-228 weight" and cost very few cycles to generate and manage. 229 The very large amounts of threads are organized into many 230 "thread blocks." The threads within a block are executed in 231 groups of 16, called a "half-warp," by the "multiprocessors" 232 (a type of vector processor), each of which executes in par-233 allel with the others. A multiprocessor can have a number of 234 "stream processors," which are sometimes called "cores." 235 A high-end Fermi GPU has 16 multiprocessors, and each 236 237 multiprocessor has two groups of 16 stream processors, which amounts to 512 processing cores. 238

239 The memory on a GPU is organized in a hierarchical structure. Each thread has access to its own register, which 240 is very fast, but the amount is very limited. The threads 241 within the same block have access to a small pool of low-242 latency "shared memory." The total amount of registers 243 and shared memory available on a GPU restricts the 244 maximum number of active warps on a multiprocessor (i.e., 245 the "occupancy"), depending upon the amount of registers 246 and shared memory used by each warp. To maximize 247 occupancy, one should minimize the usage of registers and 248 shared memory in the kernel. The most abundant memory 249 type on a GPU is the "global memory"; however, accesses 250 to the global memory have much higher latencies. To hide 251 252 the latency, one needs to launch a large number of thread blocks so that the thread scheduler can effectively overlap 253 the global memory transactions for some blocks with the 254 255 arithmetic calculations on other blocks. To reduce the total number of global memory transactions, each access needs 256 to be "coalesced" (i.e., consecutive threads accessing 257 consecutive memory addresses), otherwise the access will 258 be "serialized" (i.e., separated into multiple transactions), 259 which may heavily impact the performance of the code. 260

In addition to data-parallelism, GPUs are also capable of 261 task parallelism which is implemented as "streams" in 262 263 CUDA. Different tasks can be placed in different streams, and the tasks will proceed in parallel despite the fact that they 264 may have nothing in common. Currently task parallelism on 265 GPUs is not yet as flexible as on CPUs. Current-generation 266 NVIDIA GPUs now support simultaneous kernel executions 267 and memory copies either to or from the device. 268

3 Overview of the ADER-DG method

The ADER-DG method for solving the seismic wave 270 equation is both flexible and robust. It allows unstructured 271



272 meshes and easy control of accuracy without compromising 273 simulation stability. Like the SE method, the solution inside 274 each element is approximated using a set of orthogonal basis 275 functions, which leads to diagonal mass matrices. These 276 types of basic functions exist for a wide range of element 277 types. Unlike the SE or typical FE schemes, the solution is 278 allowed to be discontinuous across element boundaries. The 279 discontinuities are treated using well-established ideas of 280 numerical flux functions from the high-order finite-volume 281 framework. The spatial approximation accuracy can be 282 easily adjusted by changing the order of the polynomial 283 basis functions within each element (i.e., p-adaptivity). The 284 ADER time-stepping scheme is composed of three major 285 ingredients, a Taylor expansion of the degree-of-freedoms 286 (DOFs, i.e., the coefficients of the polynomial basis func-287 tions in each element) in time, the solution of the Derivative 288 Riemann Problem (DRP) (Toro and Titarev 2002) that 289 approximates the space derivatives at the element bound-290 aries and the Cauchy-Kovalewski procedure for replacing 291 the temporal derivatives in the Taylor series with spatial 292 derivatives. We summarize major equations of the ADER-293 DG method for solving the three-dimensional isotropic 294 elastic wave equation on unstructured tetrahedral meshes in 295 the following. Please refer to Dumbser and Käser (2006) for 296 details of the numerical scheme.

The three-dimensional elastic wave equation for an isotropic medium can be expressed using a first-order velocitystress formulation and written in a compact form as

$$\partial_t Q_p + A_{pq} \partial_x Q_q + B_{pq} \partial_y Q_q + C_{pq} \partial_z Q_q = 0, \qquad (1)$$

301 where O is a 9-vector consisting of the six independent components of the symmetric stress tensor and the velocity 302 vector $Q = (\sigma_{xx}, \sigma_{yy}, \sigma_{zz}, \sigma_{xy}, \sigma_{yz}, \sigma_{xz}, u, v, w)^{\mathrm{T}}$, and A_{pq}, B_{pq} 303 and C_{pq} are space-dependent 9 \times 9 sparse matrices with the 304 305 nonzero elements given by the space-dependent Lamé parameters and the buoyancy (i.e., the inverse of the density). 306 307 Summation for all repeated indices is implied in all equations. 308 The seismic source and the free-surface and absorbing 309 boundary conditions can be considered separately as shown in 310 Käser and Dumbser (2006) and Dumbser and Käser (2006).

311 Inside each tetrahedral element $T^{(m)}$, the numerical 312 solution Q_h can be expressed as a linear combination of 313 space-dependent and time-independent polynomial basis 314 functions $\Phi_I(\xi, \eta, \zeta)$ of degree N with support on $T^{(m)}$,

$$\left[\mathcal{Q}_{h}^{(m)}\right]_{p}(\xi,\eta,\zeta,t) = \hat{\mathcal{Q}}_{pl}^{(m)}(t)\Phi_{l}(\xi,\eta,\zeta),\tag{2}$$

316 where $\hat{Q}_{pl}^{(m)}(t)$ are time-dependent DOFs, and ξ , η , ζ are 317 coordinates in the reference element $T_{\rm E}$. Explicit 318 expressions for the orthogonal basis functions $\Phi_l(\xi, \eta, \zeta)$ 319 on a reference tetrahedral element are given in Cockburn 320 et al. (2000) and the appendix A of Käser et al. (2006).

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Bring Eq. (2) into Eq. (1), multiplying both sides with a test321function Φ_k , integrate over an element $T^{(m)}$, and then apply322integration by parts, we obtain,323

$$\int_{T^{(m)}} dV(\Phi_k \partial_t Q_p) + \int_{\partial T^{(m)}} dS(\Phi_k F_p^h) - \int_{T^{(m)}} dV(\partial_x \Phi_k A_{pq} Q_p + \partial_y \Phi_k B_{pq} Q_p + \partial_z \Phi_k C_{pq} Q_p) = 0.$$
(3)

The numerical flux F_p^h between the element $T^{(m)}$ and one 325 of its neighboring elements, $T^{(m_j)}$, j = 1, 2, 3, 4, can be 326 computed from an exact Riemann solver, 327

$$F_{p}^{h} = \frac{1}{2} T_{pq}^{j} \left(A_{qr}^{(m)} + \left| A_{qr}^{(m)} \right| \right) (T_{rs}^{j})^{-1} \hat{Q}_{sl}^{(m)} \Phi_{l}^{(m)} + \frac{1}{2} T_{pq}^{j} \left(A_{qr}^{(m)} - \left| A_{qr}^{(m)} \right| \right) (T_{rs}^{j})^{-1} \hat{Q}_{sl}^{(m_{j})} \Phi_{l}^{(m_{j})},$$
(4)

where T_{pq}^{j} is the rotation matrix that transforms the vector 329 Q from the global Cartesian coordinate to a local normal 330 coordinate that is aligned with the boundary face between 331 the element $T^{(m)}$ and its neighbor element $T^{(m_j)}$. Bring Eq. 332 (4) into Eq. (3) and convert all the integrals from the global 333 xyz-system to the $\xi \eta \zeta$ -system in the reference element $T_{\rm E}$ 334 through a coordinate transformation, we obtain the semi-335 discrete discontinuous Galerkin formulation, 336

$$J|\hat{o}_{l}\hat{Q}_{pl}^{(m)}M_{kl} - |J| \left(A_{pq}^{*}\hat{Q}_{ql}^{(m)}K_{kl}^{\xi} + B_{pq}^{*}\hat{Q}_{ql}^{(m)}K_{kl}^{\eta} + C_{pq}^{*}\hat{Q}_{ql}^{(m)}K_{kl}^{\zeta}\right) + \frac{1}{2}T_{pq}^{j} \left(A_{qr}^{(m)} + \left|A_{qr}^{(m)}\right|\right) (T_{rs}^{j})^{-1}\hat{Q}_{sl}^{(m)}F_{kl}^{-j} + \frac{1}{2}T_{pq}^{j} \left(A_{qr}^{(m)} - \left|A_{qr}^{(m)}\right|\right) (T_{rs}^{j})^{-1}\hat{Q}_{sl}^{(m)}F_{kl}^{+j,i,h} = 0, \quad (5)$$

where |J| is the determinant of the Jacobian matrix of the 338 coordinate transformation being equal to 6 times the 339 volume of the tetrahedron, $|S_i|$ is the area of face *j* between 340 the element $T^{(m)},$ and its neighbor element $T^{(m_j)},$ $A_{pq}^*,$ B_{pq}^* , 341 and C_{pq}^* are linear combinations of A_{pq} , B_{pq} , and C_{pq} with 342 the coefficients given by the Jacobian of the coordinate 343 transformation, M_{kl} , K_{kl}^{ξ} , K_{kl}^{η} , and K_{kl}^{ζ} are the mass, stiffness, 344 and flux matrices are given by 345

$$F_{kl}^{-j} = \int_{\partial(T_{\mathrm{E}})_j} [\boldsymbol{\Phi}_k(\boldsymbol{\xi}^{(j)}(\boldsymbol{\chi}, \tau)) \boldsymbol{\Phi}_l(\boldsymbol{\xi}^{(j)}(\boldsymbol{\chi}, \tau))] \mathrm{d}\boldsymbol{\chi} \mathrm{d}\boldsymbol{\tau},$$

$$\forall 1 \le j \le 4,$$
(6)

$$F_{kl}^{+,j,i,h} = \int_{\partial(T_{\rm E})_j} \left[\Phi_k(\xi^{(j)}(\chi,\tau)) \Phi_l(\xi^{(i)}(\tilde{\chi}^{(h)}(\chi,\tau), \tilde{\tau}^{(h)}(\chi,\tau))) \right] \qquad 347$$
$$d\chi d\tau \quad \forall 1 \le i \le 4, \forall 1 \le h \le 3.$$
(7)

The mass, stiffness, and flux matrices are all computed 349 on the reference element which means that they can be 350

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- 351 evaluated analytically beforehand using a computer algebra
- 352 system (e.g., Maple, Mathematica) and stored on disk.
- 353 If we project Eq. (1) onto the DG spatial basis functions,
- the temporal derivative of the DOF can be expressed as

$$\partial_t \hat{Q}_{pn}(t) = (-M_{nk}^{-1} K_{lk}^{\zeta} A_{pq}^* - M_{nk}^{-1} K_{lk}^{\eta} B_{pq}^* - M_{nk}^{-1} K_{lk}^{\eta} C_{pq}) \hat{Q}_{ql}(t),$$

and the *m*-th temporal derivative can be determinedrecursively as

$$\partial_t^m \hat{Q}_{pn}(t) = (-M_{nk}^{-1} K_{lk}^{\xi} A_{pq}^* - M_{nk}^{-1} K_{lk}^{\eta} B_{pq}^* - M_{nk}^{-1} K_{lk}^{\zeta} C_{pq}^*) \partial_t^{m-1} \hat{Q}_{ql}(t).$$
(8)

359 The Taylor expansion of the DOF at time t^n is,

$$\hat{\mathcal{Q}}_{pn}(t) = \sum_{m=0}^{N} \frac{(t-t^n)^m}{m!} \partial_t^m \hat{\mathcal{Q}}_{pn}(t^n),$$

361 which can be integrated from t^n to t^{n+1} ,

$$I_{pnql}(\Delta t)\hat{Q}_{ql}(t^{n}) \equiv \int_{t^{n}}^{t^{n+1}} \hat{Q}_{pn}(t)dt = \sum_{m=0}^{N} \frac{\Delta t^{m+1}}{(m+1)!} \partial_{t}^{m} \hat{Q}_{pn}(t^{n}),$$
(9)

363 where $\Delta t = t^{n+1} - t^n$, and $\partial_t^m \hat{Q}_{pn}(t^n)$ can be computed 364 recursively using Eq. (8).

365 Considering Eq. (9), the fully discretized system can 366 then be obtained by integrating the semi-discrete system, 367 Eq. (5), from t^n to t^{n+1} ,

$$\begin{split} J &|[\hat{Q}_{pl}^{(m)n+1} - \hat{Q}_{pl}^{(m)n}]M_{kl} \\ &= |J|(A_{pq}^{*}K_{kl}^{\xi} + B_{pq}^{*}K_{kl}^{\eta} + C_{pq}^{*}K_{kl}^{\zeta})I_{qlmn}(\varDelta t)(\hat{Q}_{mn}^{(m)})^{n} \\ &- \frac{1}{2}\sum_{j=1}^{4} |S_{j}|T_{pq}^{j}\left(A_{qr}^{(m)} + \left|A_{qr}^{(m)}\right|\right)\left(T_{rs}^{j}\right)^{-1}F_{kl}^{-j}I_{slmn}(\varDelta t)(\hat{Q}_{mn}^{(m)})^{n} \\ &- \frac{1}{2}\sum_{j=1}^{4} |S_{j}|T_{pq}^{j}\left(A_{qr}^{(m)} - \left|A_{qr}^{(m)}\right|\right)\left(T_{rs}^{j}\right)^{-1}F_{kl}^{+,j,i,h}I_{slmn}(\varDelta t)(\hat{Q}_{mn}^{(m)})^{n}. \end{split}$$

$$(10)$$

Equation (10), together with Eqs. (8) and (9), provides
the mathematical foundation for our GPU implementation
and optimization.

372 4 Implementation and optimization on multiple GPUs

Prior to running our wave-equation solver, a tetrahedral
mesh for the entire modeling domain was generated on a
CPU using the commercial mesh generation software
"GAMBIT." The mesh generation process is fully automated, and the generated tetrahedral mesh conforms to all
discontinuities built into the modeling geometry, including

4.1 Pre-processing 385

In Fig. 1, we listed the major steps in the reference parallel 386 CPU code, "SeisSol" la Puente De et al. (2009), and those 387 in our parallel CPU-GPU hybrid implementation. In our 388 parallel CPU-GPU hybrid implementation, we assume that 389 each MPI process has access to only one device, and each 390 device is controlled by only one MPI process. At the start 391 of the calculation, a sequence of pre-processing steps is 392 executed on the CPUs. The pre-processing sequence 393 includes: 394

- (1) reading and processing a control file;
- (2) reading and processing geometric information, which include the tetrahedral mesh, the boundary conditions, the material properties (i.e., density and Lamé parameters) for each element, and the mesh partitioning information generated by METIS;
 (2) reading and processing geometric information, which 396 397 397 397 398 399 400
- (4) reading and processing the DG matrices, which 406 include the mass, stiffness, and flux matrices, which 407 were pre-computed and stored on the disk; and 408
- (5) reading and processing the files describing the seismic 409 source and seismic receivers. 410

Our CUDA program adopts the typical CUDA pro-411 gramming model. After the pre-processing sequence is 412 carried out on the host CPUs, the arrays needed by the 413 CUDA kernels are then copied to the global memory of the 414 devices using "cudaMemcpy." The hosts then call a 415 sequence of CUDA kernels in every time step. The results 416 of the simulation (e.g., the synthetic seismograms) are 417 stored on the devices during the time loop and copied back 418 419 to the hosts after all time steps are completed.

In our implementation, the calculation for each tetra-420 hedral element is carried out by one thread block. Within 421 each thread block, the number of threads depends upon the 422 dimension of the element's DOFs. The DOFs, $\hat{Q}_{pl}^{(m)}$, are 423 allocated and initialized in the global memory of the device 424 using "cudaMalloc" and "cudaMemset." For a 5th-order 425 426 scheme which is sufficiently accurate for most of our applications, the number of DOFs per component per 427

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GPU assemble message and copy to host

CPU non-blocking MPI

GPU copy message from host and distribute



Fig. 1 The flowcharts of the major steps in the reference parallel CPU codes (left) and those in our CPU-GPU hybrid implementation (right). The whole calculation can be separated into three sections: pre-processing, time-stepping, and post-processing. The pre-processing section reads and calculates all the data that the time-stepping section will use. The time-stepping section updates the DOFs of each tetrahedral element according to Eqs. (8)-(10) and has been ported to the GPU. The post-processing section is in charge of writing out the DOFs and/or the seismograms at the pre-specified locations

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428 element is 35. Considering the nine components of the 429 governing PDE (i.e., six stress components and three 430 velocity components), the DOFs of each element consist of 431 a 9 \times 35 matrix which is represented in memory as a one-432 dimensional array of length 315 organized in the column-433 major ordering. To obtain better memory alignment, we 434 padded five zeros behind the DOFs of each element so that 435 the length of the one-dimensional DOF array of each ele-436 ment is increased to 320, which is 10 times the number of 437 threads in a warp. For a subdomain of "nElem" elements, 438 the length of the one-dimensional DOF array for the whole 439 subdomain is, therefore, "nElem \times 320." The amount of 440 memory that is wasted on purpose is less than 1.6 %; 441 however, the better memory alignment improved the per-442 formance of some simple operations such as summation 443 operations and scalar-product operations by around 6.3 %.

444 4.2 Matrix-matrix multiplications

445 The implementation and optimization details for steps (1)–(5)446 are documented in Mu et al. (2013). In this section, we give a 447 very brief summary. In those steps, most of the total wall-time 448 is spent on matrix-matrix multiplications. We use step (2) 449 which computes the volume contribution, as an example. A 450 flowchart of the major calculations in step (2) is shown in 451 Fig. 2a. Considering the first term on the right-hand-side of 452 Eq. (10), the calculations in step (2) involve mathematical operations in the form of $A_{pq}^* K_{kl}^{\xi} [I_{qlmn}(\Delta t) (\hat{Q}_{mn}^{(m)})^n]$, where the 453 time-integrated DOF $I_{qlmn}(\Delta t)(\hat{Q}_{mn}^{(m)})^n$, denoted as "dgwork" 454 455 in Fig. 2a, is computed in step (1) and has the same dimension 456 and memory layout as the DOF array. The multiplication between K_{kl}^{ξ} , denoted as "Kxi" in Fig. 2a, and the time-457 458 integrated DOF is different from the normal matrix-matrix 459 product in linear algebra. This multiplication involves three 460 steps: first, transpose the time-integrated DOF matrix, second, 461 multiply with the stiffness matrix following the usual matrix-462 matrix product rule, third, transpose the matrix obtained in the 463 previous step. We call this multiplication the "left-multipli-464 cation." A code segment for the baseline CUDA implemen-465 tation of the left-multiplication is shown in Fig. 2b. This left-466 multiplication operation is used extensively through the cal-467 culations in steps (1)-(4) and deserves more optimization 468 effort. First, we can reduce the number of floating-point 469 operations by exploiting the fact that some of the matrices in 470 this operation are sparse; second, the order of the floating-471 point operations can be rearranged in a way such that the 472 accesses to "dgwork" in the global memory are as coalesced 473 as possible. The DOF, its temporal derivatives, and the time-474 integrated DOF are generally dense. However, the stiffness 475 matrices and the Jacobians have fill-ratios ranging from 8.8 % 476 to 29.6 %. To take advantage of this sparsity, one possibility

is to adopt an existing sparse linear algebra library such as 477 478 "CUSP" (Bell and Garland 2009) or cuSPARSE. However, the result we obtained using "CUSP" was not very satisfac-479 tory. The best performance gain, which was obtained using 480 the "HYB" matrix format, was about 36.2 % compared with 481 482 the baseline implementation shown in Fig. 2b. This is largely due to the very irregular distribution of the non-zeros in our 483 matrices, which caused a large number of uncoalesced 484 accesses to the time-integrated DOF arrays, and the amount of 485 486 arithmetic calculations was not large enough to hide the 487 memory access latencies due to the low fill-ratio in the stiffness matrix. Considering the fact that the locations of the non-488 489 zero elements in the stiffness matrices can be determined beforehand and are fixed throughout the program, the results 490 of the left-multiplications can be evaluated analytically 491 492 beforehand and expressed in terms of the non-zero elements in those matrices using a computer algebra system. The 493 494 expressions of the left-multiplication results, which are linear combinations of the time-integrated DOF with coefficients 495 given by the non-zero elements of the stiffness matrices, can 496 497 be hardwired into the CUDA kernels. This implementation 498 eliminates all redundant calculations involving zero elements and by carefully arranging the order of the calculations in 499 accordance with the thread layout, we can also minimize the 500 number of uncoalesced memory accesses to the time-inte-501 grated DOF array. A code segment of the optimized left-502 multiplication is shown in Fig. 2c, which is about 4 times 503 504 faster than the baseline implementation shown in Fig. 2b. This approach can also be applied to normal matrix-matrix 505 product and is used throughout steps (1)-(4) in our optimized 506 507 CUDA codes. A drawback of this approach is that the resulting kernel source code is quite long, and some manual 508 editing is required to ensure coalesced memory accesses. 509 510 However, modern computer algebra systems (e.g., Mathematica, Maple) usually have automated procedures for trans-511 lating long mathematical expressions into the C language 512 which is usually error-proof and can be directly incorporated 513 into the CUDA kernels with minimal effort. 514

515 Our own matrix-matrix multiplication scheme greatly 516 contributes our CUDA codes. Before we settled for the final version of our single-GPU code, we also complete two 517 other versions of CUDA implementations, one is the 518 baseline implementation, which adapts conventional 519 CUDA dense matrix-matrix multiplication, and the other is 520 521 the median implementation which uses sparse matrix-522 matrix multiplication scheme. As a result, compared with the CPU based ADER-DG code, the baseline implemen-523 tation obtains a speedup factor of $9.7 \times$, and the median 524 implementation improved the speedup factor from $9.7 \times$ to 525 13.2×. This improvement mainly gains from getting rid of 526 all zeros elements' computation; however, due to the very 527 irregular distribution of non-zeros locality, this median 528



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(b)

```
_global__void original_kxi_dgwork_multiply(float* temp_DOF, float* Kxi_dense, float* dgwork)
{
    int iblock = blockIdx.x;
    int irow = threadIdx.x; // 0-34
    int icol = threadIdx.y; // 0-8
    float temp = 0.0;
    for (int i=0; i<35; i++) {
        temp += dgwork[iblock*9*35 + icol*35 + i] * Kxi_dense[i*35 + irow];
    }
    temp_DOF[iblock*9*35 + icol*35 + irow] += temp;
}</pre>
```

(c)

```
_global__ void optimize_kxi_dgwork_multiply(float* temp_DOF, float* Kxi_sparse, float* dgwork)
{
      int iblock = blockIdx.x;
                                  // 0-8
      int irow = threadIdx.x;
      // temp_DOF[iblock*320 + 0 + irow] += 0; // no need to calculate
                                                                                                          // COL 1
        temp_DOF[iblock*320 + 9 + irow] += dgwork[iblock*320 + 0 + irow] * Kxi_sparse[0 + irow];
                                                                                                          // COL 2
      // temp_DOF[iblock*320 + 18 + irow] += 0; // no need to calculate
                                                                                                          // COL 3
      // temp DOF[iblock*320 + 27 + irow] += 0; // no need to calculate
                                                                                                          // COL 4
        temp_DOF[iblock*320 + 36 + irow] += dgwork[iblock*320 + 9 + irow] * Kxi_sparse[9 + irow];
                                                                                                         // COL 5
        temp_DOF[iblock*320 + 45 + irow] += dgwork[iblock*320 + 0 + irow] * Kxi_sparse[18 + irow] +
                                                                                                         // COL 6
                                              dgwork[iblock*320 + 18 + irow] * Kxi_sparse[27 + irow] +
                                              dgwork[iblock*320 + 27 + irow] * Kxi_sparse[36 + irow];
```

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✓ Fig. 2 a The flowchart of the calculations in step (2), the volume contributions. "dudt" is the volume contribution, "Kxi," "Keta," "Kzeta" correspond to the stiffness matrices, K_{lk}^{ζ} , K_{lk}^{η} , K_{lk}^{ζ} , in the text. "JacobianDet" is the determinant of the Jacobian |J|. "nElem" is the number of tetrahedral elements in the subdomain, "nDegFr" is the number of DOFs per component per tetrahedral element, "nVar" is the number of components in the governing equation. "AStar," "BStar," "CStar" correspond to A^* , B^* , C^* in the text. Code segments for the calculations in the dark-gray box are listed in b and c. b. Baseline implementation of the CUDA kernel for the "leftmultiplication" between the time-integrated DOF and the stiffness matrix K_{μ}^{ζ} . "Kxi_dense" corresponds to the dense matrix representation of K_{μ}^{ζ} , "dgwork" corresponds to the time-integrated DOF, and the result of the multiplication is stored in "temp_DOF." c A segment of the optimized CUDA kernel for the "left-multiplication" between the time-integrated DOF and the stiffness matrix K_{lk}^{ζ} . "Kxi_sparse" corresponds to the sparse matrix representation of K_{lk}^{ζ} . Meanings of other symbols are identical to those in Fig. b

529 implementation still almost 2 times slower than our final 530 implementation, which enjoys a speedup factor of $24.3 \times$.

531 4.3 Overlapping communication with computation

532 Considering Eqs. (8)–(10), the calculations on the devices 533 within each time step can be organized into five major steps:

- 534 (1) calculating the time-integrated DOFs, i.e., the term 535 $I_{qlmn}(\Delta t)(\hat{Q}_{mn}^{(m)})^n$ using the DOFs $(\hat{Q}_{mn}^{(m)})^n$ at the 536 current time step through the Cauchy-Kovalewski 537 procedure, i.e., Eqs. (8) and (9),
- (2) calculating the volume contributions, i.e., the first
 term on the right-hand-side of Eq. (10), using the
 time-integrated DOFs obtained in step (1),
- 541 (3) calculating the first numerical flux term, i.e., the
 542 second term on the right-hand-side of Eq. (10), using
 543 the time-integrated DOFs obtained in step (1),
- (4) calculating the second numerical flux term, i.e., the
 third term on the right-hand-side of Eq. (10), using
 the time-integrated DOFs of the four neighboring
 elements obtained in step (1),
- 548 (5) updating the DOFs to the next time step $(\hat{Q}_{pl}^{(m)})^{n+1}$ 549 using the DOFs at the current time step $(\hat{Q}_{pl}^{(m)})^n$, the 550 volume contributions obtained in step (2) and the 551 numerical flux terms obtained in steps (3) and (4), as 552 well as any contributions from the seismic source, by 553 using Eq. (10) which also involves inverting the mass 554 matrix M_{kl} , which is diagonal.

All the calculations in steps (1), (2), (3), and (5) can be performed in an element-local way and require no interelement information exchange, which is ideal for SIMDtype processors such as GPUs. The calculations in step (4) need to use the time-integrated DOFs from all neighboring elements which in our distributed-memory, parallel implementation requires passing time-integrated DOFs of
the outer elements of each subdomain across different MPI
processes. Most of this communication overhead can be
hidden through overlapping computation with
communication.561
562563

566 In our implementation, we calculate the time-integrated DOFs for all the outer elements of a subdomain first. The 567 calculation of the time-integrated DOF requires access to 568 the DOF array in the global memory. The DOFs of the 569 570 outer elements are usually scattered throughout the entire 571 DOF array of the subdomain. To avoid non-coalesced memory accesses, which could impact performance by up 572 573 to 54 %, the entire DOF array is split into two sub-arrays, one for DOFs of all the outer elements and the other for the 574 DOFs of all inner elements. Once we complete the calcu-575 576 lations of the time-integrated DOFs of the outer elements, the device starts to compute the time-integrated DOFs of 577 the inner elements of the subdomain right away. At the 578 same time, the time-integrated DOFs of the outer elements 579 are assembled into a separate array which is then copied 580 581 into the host memory asynchronously to fill the MPI buffer 582 using a separate CUDA stream, and then the host initiates a non-blocking MPI data transfer and returns. While the 583 messages are being transferred, the device completes the 584 calculations of the time-integrated DOFs of the inner ele-585 ments, combines them with the time-integrated DOFs of 586 587 the outer elements into a single time-integrated DOF array and proceeds to calculations of the volume contributions in 588 step (2) and the first numerical flux term in step (3). On the 589 host, synchronization over all the MPI processes is per-590 591 formed; once the host receives the array containing the time-integrated DOFs of the outer elements on the neigh-592 boring subdomains, it is copied to the device asynchro-593 594 nously using a separate CUDA stream. After completing 595 step (3), the device synchronizes all streams to make sure that the required time-integrated DOFs from all neighbor-596 ing subdomains have arrived and proceed to calculate the 597 598 second numerical flux term in step (4) and then update the 599 DOFs as in step (5). The overhead for splitting the entire 600 DOF array into two sub-arrays for inner and outer elements and for combining the time-integrated DOFs of the outer 601 and inner elements into a single array amounts to less than 602 603 0.1 % of the total computing time on the device. The entire process is illustrated in Fig. 1. 604

605 There are many factors can influent the speedup factor contribution by overlapping communication with compu-606 tation; the overlapping benefit almost differs from com-607 puter to computer. Based on our completed experiments, 608 609 the best scenario which all the GPUs located on the same 610 node, the communication time takes 11.7 % of total computation time, while when each GPU locate on the different 611 node, the ratio could rise up to 25.1 %. However, since we 612 613 apply the multiple streams and the overlapping techniques,

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614 the overhead caused by communication could be 615 eliminated.

To ensure effective communication-computation over-616 617 lap, the ratio of the number of the outer to inner elements 618 must be sufficiently small. An upper bound of this ratio can 619 be estimated based on both the processing capability of the 620 devices and the speed of the host-device and host-host 621 inter-connections. On the NVIDIA Fermi M2070 GPUs 622 that we experimented with, we achieved nearly zero 623 communication overheads when this ratio is below 2 %. 624 We note that if the same approach is implemented using a 625 classic CPU cluster, this ratio can be much larger, since the calculations for the inner elements and steps (2) and (3) are 626 627 over an order of magnitude slower on a CPU core.

628 **5** Performance analysis

629 In this study, the speedup factor is defined as the ratio 630 between the wall-time spent on running a simulation on a number of CPU cores with the wall-time spent on running 631 632 the same simulation on the same or less number of GPUs. 633 The CPU used as the reference is the Intel Xeon W5660 (2.80 GHz/12 MB L2 cache) processor, and the GPU is the 634 635 NVIDIA Tesla C2070 (1.15 GHz/6 GB 384bit GDDR5) 636 processor. Specifications of our CPU and GPU processors can be found on Intel and NVIDIA's websites. 637

638 The speedup factor depends strongly upon how well the 639 reference CPU code is optimized and sometimes also on 640 the specific CPU compiler and compiling flags. The fastest 641 executable on our CPU was obtained using the Intel compiler "ifort" with the flag "-O3." The wall-time for 642 643 running the CPU code in double-precision mode is only 644 slightly longer than running the CPU code in single-precision mode by around 5 %. Our GPU codes were com-645 piled using the standard NVIDIA "nvcc" compiler of 646 647 CUDA version 4.0. Throughout this article, we use the 648 double-precision version of the fastest CPU code as the 649 reference for computing the speedup factors of our single-650 and double-precision GPU codes.

The accuracy of our single-precision GPU codes is 651 sufficient for most seismological applications. The com-652 653 puted seismograms have no distinguishable differences 654 from the seismograms computed using the double-preci-655 sion version of the reference CPU code, and the energy of 656 the waveform differences is much less than 1 % of the total 657 energy of the seismogram.

659 For our single-GPU performance analysis, we computed 660 the speedup factors for problems with seven different mesh 661 sizes (Fig. 3). The number of tetrahedral elements used in

5.1 Single-GPU performance

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our experiments is 3,799, 6,899, 12,547, 15,764, 21,121, 662 24,606, and 29,335. The material property is constant 663 throughout the mesh with density 3,000 kg/m³ and Lamé 664 parameters $\lambda 5.325 \times 10^{10}$ and $\mu 3.675 \times 10^{10}$ Pascal. We 665 applied the traction-free boundary condition on the top of 666 the mesh and absorbing boundary condition on all other 667 boundaries. The seismic source is an isotropic explosive 668 source buried in the center of the mesh. The wall-time 669 measurements were obtained by running the simulations 670 671 for 1,000 time steps. The speedup factors were computed for our single-precision GPU code with respect to the CPU 672 code running on one, two, four, and eight cores. For the 673 multi-core runs on the CPUs, the parallel version of the 674 "SeisSol" code is used as the reference. For the seven 675 different mesh sizes, the speedup factor ranges from 23.7 to 676 25.4 with respect to the serial CPU code running on one 677 core, from 12.2 to 14 with respect to the parallel CPU code 678 running on two cores, from 6.5 to 7.2 with respect to the 679 parallel CPU code running on four CPU cores, and from 680 3.5 to 3.8 with respect to the parallel CPU code running on 681 eight CPU cores. The speedup factor does not decrease 682 linearly with increasing number of CPU cores. For 683 instance, the speedup factor with respect to eight CPU 684 cores is about 14 % better than what we would have 685 expected considering the speedup factor with respect to one 686 CPU core if we had assumed a linear scaling. For the 687 parallel version of the CPU code, there are overheads 688 incurred by the MPI communication among different cores, 689 while for the single-GPU simulations, such communication 690 overheads do not exist. 691

692 Since most of the calculations in the ADER-DG method are carried out in an element-local way, and there are no 693 inter-process communication overheads on a single GPU, 694 we expect the "strong scaling" on a single GPU, defined as 695 the total wall-time needed to run the application on one 696 GPU when the total number of elements (i.e., the amount 697 of workload) is increased (e.g., Michéa and Komatitsch 698 699 2010), to be nearly linear. In Fig. 4, we show the total wall-700 time for 100 time steps as a function of the total number of 701 tetrahedral elements. As we can see, the strong scaling of 702 our codes on a single GPU is almost linear. The calculations in step (4) (i.e., the second term in the numerical flux) 703 involve time-integrated DOFs of direct neighbors; how-704 ever, this inter-element dependence keeps its spatially local 705 character, while the number of elements increases and does 706 707 not affect the scaling.

5.2 Multiple-GPU performance 708

To analyze the performance of the parallel version of our 709 CUDA codes, we use a simplified version of the SEG/ 710 711 EAGE salt model (Käser et al. 2010) as the benchmark. This model is geometrically complex, as shown in Fig. 5a 712

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Fig. 3 Single-GPU speedup factors obtained using 7 different meshes and 4 different CPU core numbers. The total number of tetrahedral elements in the 7 meshes is 3,799, 6,899, 12,547, 15,764, 21,121, 24,606, and 29,335, respectively. The speedup factors were obtained by running the same calculation using our CPU-GPU hybrid code with 1 GPU and using the serial/parallel "SeisSol" CPU code on 1/2/4/8 CPU cores on the same compute node. The black columns represent the speedup of the CPU-GPU hybrid code relative to 1 CPU core, the dark-gray columns represent the speedup relative to 2 CPU cores, the light gray column represents the speedup relative to 4 CPU cores and the lightest gray columns represent the speedup relative to 8 CPU cores



Fig. 4 Strong scalability of our single GPU code with different mesh sizes. The black squares show the average wall-time per 100 time steps, and the number of elements varies from 800 to 57,920

and b. However, the generation of the tetrahedral mesh for
such a complex model is highly automatic, once the
geometries of the structural interfaces are imported into the
meshing software. The material properties of the different
zones in this model are summarized in Table 1. We note

that a thin layer of water lies on top of the three-dimen-
sional model. The ADER-DG method can accurately718handle seismic wave propagation in water simply by set-
ting the shear modulus of the elements in the water region720to zero (Käser and Dumbser 2008).722

723 This salt model is discretized into tetrahedral meshes 724 with different number of elements. In Fig. 6, we show the speedup factors obtained for two different mesh sizes, one 725 with 327,886 elements, and the other with 935,870 ele-726 ments. The simulations were run on 8, 16, 32, and 48 CPU 727 cores using the parallel version of the "SeisSol" code. And 728 the speedup factors were obtained by running the same 729 simulations on the same number of GPUs. On average, the 730 speedup factor for our parallel GPU codes is around 28, 731 732 which is slightly higher than the speedup factor obtained in the single-GPU-single-CPU comparison. This may due to 733 the fact that in the parallel CPU code, the outer elements of 734 a subdomain are not treated separately from the inner 735 elements, which do not allow the parallel CPU code to 736 overlap the computation on the inner elements with the 737 communication of the time-integrated DOFs of the outer 738 elements. 739

To investigate the strong scalability (i.e., the decrease in 740 wall-time with increasing GPU number, while holding the 741 total workload that is the number of elements and time 742

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Fig. 5 a A perspective view of the 3D geometry of the discretized salt body in the SEG/EAGE salt model. b A two-dimensional cross-section view of the SEG/EAGE salt model along the A-A' profile (Aminzadeh et al. 1997). The material properties for the different geological structures are listed in Table 1

	$\rho ~({\rm kg/m^3})$	λ (10 ⁹)	<i>M</i> (Pa 10 ⁹)	$V_{\rm p}~({\rm m/s})$	$V_{\rm s}$ (m/s)
Water	1,020	2.2950	0	1,500	0
Zone 01	2,000	4.5067	4.5067	2,600	1,501
Zone 02	2,050	5.0000	5.0000	2,705	1,562
Zone 03	2,500	7.5000	7.5000	3,000	1,732
Zone 04	2,600	9.0000	9.0000	3,223	1,861
Salt	2,160	20.800	14.457	5,094	3,103

Table 1 Material property of the SEG 3D salt model example

743 steps, constant), we discretized the salt model using a mesh 744 with about 1.92 million elements and ran the simulation for 745 100 times steps. The number of GPUs used in the simu-746 lations ranges from 32 to 64. As seen on Fig. 7, the strong 747 scaling of our parallel GPU codes is close to the ideal case 748 with some fluctuations. Our codes start to slightly under-749 perform the ideal case when the number of GPUs used in 750 the simulation is larger than 48. As analyzed in Sect. 4.2, to 751 effectively overlap computation with communication, the 752 ratio between the number of outer elements and the number 753 of inner elements of a subdomain cannot exceed a certain 754 threshold, which is determined by the processing capability

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of the GPU and the speed of the inter-connections. In our case, when the number of GPUs used in the simulation 756 starts to exceed 48, this ratio becomes larger than 2 %, 757 which we believe is the threshold for our hardware con-758 759 figuration. The performance of our parallel GPU codes depends upon a number of factors, such as load balancing, 760 but we think the extra communication overhead that was 761 not effectively hidden by the computation was the domi-762 nant factor for causing our codes to underperform the ideal 763 case. In Fig. 8, we show the results of our weak scaling test 764 765 (i.e., the workload per GPU is kept about constant while increasing the number of GPUs). By definition, the total 766 number of elements in the weak scaling test increases 767 approximately linearly with the number of GPUs. If the 768 769 communication cost is effectively overlapped by computation, the weak scaling test should be approximately flat. 770 771 In our tests, the average number of elements per GPU was kept around 53,000 with about 6 % fluctuation across dif-772 ferent simulations. The ratio between the number of outer 773 and inner elements was kept around 1 %. The weak scaling 774 775 is approximately flat (Fig. 8), with some fluctuation mostly caused by the variation in the number elements per GPU 776 used in each simulation. 777



Fig. 6 Speedup factors of our parallel GPU codes obtained using two different mesh sizes. The number of tetrahedral elements used in our experiments are 327,866, 935,870. The speed factors were computed for our single-precision multiple-GPUs code with respect to the CPU code running on 16/32/48/64 cores runs on different nodes



Fig. 7 Strong scalability of our multiple-GPUs codes with 1.92 million elements, the black line shows the average wall-time per 100 time steps for this size-fixed problem performed by 32–64 GPUs

778 5.3 Application examples

We have applied our multiple-GPUs code on two welldefined models, one is the SEG-EAGE Salt, and the other
is marmousi2. All the results with these two models have
been compared with CPU code SeisSol for validation.

For the marmousi2 model, we extrude its 2D original profile and make it a 3D model with dimension of 3,500 m in depth, 17,000 m in length, and 7,000 m in width (Fig. 9a). There are 379,039 tetrahedral elements, and each element has its own material property, also 337 receivers



Fig. 8 Weak scalability of our multiple-GPUs code performed by 2–80 GPUs, the black line shows the average wall-time per 100 time steps for these size-varied problems. The average number of elements per GPU is around 53,000 with about 6 % fluctuation

locate at 5 m beneath the surface along the A-A' (yellow) 788 789 line, and the horizontal interval is 50 m; the explosive 790 source located at 10.0 m(depth), 7,500.0 m(length), 3,500.0 m(width). In this case, we used 16 M2070 Fermi 791 GPUs located on eight different nodes, and each node has 2 792 GPUs. Our CUDA code uses 16 GPUs spend 4,812.64(s) to 793 calculate 5 s seismogram, (Fig. 9b), while the SeisSol runs 794 795 on 16 CPU cores need 135,278.50 s, the speedup factor of 28.11×. 796

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Fig. 9 a A perspective view of the 3D Marmousi2 model with dimension of 3,500 m in depth, 17,000 m in length, and 7,000 m in width. There are 379.039 tetrahedral elements, and each element has its own material property. There are 337 receivers locate at 5 m beneath the surface along the A-A' (yellow) line, and the horizontal interval is 50 m; the explosive source located at 10.0 m(depth), 7,500.0 m(length), 3,500.0 m(width). (b). The plot of the marmousi2 model shot gather, computed by our multiple-GPUs code. Our CUDA code uses 16 GPUs spend 4,812.64(s) calculate 5 s seismogram, while the SeisSol runs on 16 CPU cores need 135,278.50(s), it's a speedup of 28.11×. (Color figure online)

797 For the SEG/EAGE salt model, we remove the very 798 detailed original structure and only keep the main features, 799 such as the salt body and those main faults (Fig. 10a). This 800 simplified SEG/EAGE salt model with dimension of 4,200 m 801 in depth, 13,500 m in length, and 13,500 m in width. The total 802 tetrahedral elements number is 447,624; each element has its 803 own material property. There are 192 receivers locate at 5 m 804 beneath the surface along A-A' (yellow) line, and the hori-805 zontal interval is 50 m; the explosive source located at 806 10.0 m(depth), 7,060.0 m(length), 4,740.0 m(width). In this 807 case, we used the same hardware we used for the marmousi2 808 model. Our CUDA code uses 16 GPUs spend 7,938.56 s 809 calculate 7 s seismogram, (Fig. 10b) while the SeisSol runs 810 on 16 CPU cores need 224,589.80 s, it's a speedup of $28.29 \times$.

811 **6** Summary

812 In this study, we have successfully ported the ADER-DG 813 method for solving the three-dimensional isotropic elastic 814 seismic wave equation on unstructured tetrahedral meshes 815 to CPU-GPU hybrid clusters using NVIDIA's CUDA pro-816 graming model and the message-passing interface (MPI). 817 The serial version of our CUDA codes runs approximately 818 24.3 times faster than the reference serial CPU codes at 819 single precision and about 12.8 times at double precision.

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The parallel version of our CUDA codes runs about 28.3 820 times faster than the reference parallel CPU codes at single 821 precision and about 14.9 times at double precision. The 822 increase in speed can be directly translated into an increase 823 824 in the size of the problems that can be solved using the 825 ADER-DG method. Some preliminary performance analysis shows that our parallel GPU codes have favorable 826 strong and weak scalability as long as the ratio between the 827 number of outer elements and inner elements of each sub-828 domain is smaller than a certain threshold. 829

The ADER-DG method has a number of unique charac-830 teristics that make it very suitable for acceleration using 831 GPU-type SIMD processors. The majority of the calcula-832 tions can be carried out in an element-local way with weak 833 inter-element coupling implemented using the numerical 834 835 flux functions. In particular, as shown in Eq. (10), the only term that involves inter-element information exchange is the 836 second term in the numerical flux, and we have shown that 837 838 on a distributed-memory parallel system, the communication cost can be effectively overlapped with computation. 839 This locality in the ADER-DG method makes it relatively 840 straightforward to partition the workload among different 841 thread blocks on each GPU and also among different GPUs 842 on the cluster and results in close-to-ideal scalability. The 843 ADER-DG method is also a high-order method, which 844 requires more work per DOF than low-order methods. The 845

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Fig. 10 a A perspective view of the simplified SEG/EAGE salt model with dimension of 4,200 m in depth, 13,500 m in length and 13,500 m in width. There are 447,624 tetrahedral elements and each element has its own material property. There are 192 receivers locate at 5 m beneath the surface along A-A' (yellow) line and the horizontal interval is 50 m, the explosive source located at 10.0 m (depth), 7,060.0 m (length), 4,740.0 m (width). b The plot of the SEG/EAGE salt model shot gather, computed by our multiple-GPUs code. Our CUDA code uses 16 GPUs spend 7,938.56(s) calculate 7 s seismogram, while the SeisSol runs on 16 CPU cores need 224,589.80(s), it's a speedup of 28.29×. (Color figure online)

846 increase in arithmetic intensity shifts the bottleneck from the

- 847 memory bandwidth to the compute bandwidth. The relative 848
- abundance of cheap computing power on a GPU makes it
- 849 favorable for implementing high-order methods.

850 7 Discussion

851 Debates still exist in the computer sciences community 852 about how the speedup factor should be defined in a more 853 general and objective way. Some definitions are more 854 favorable to the GPUs, and some definitions are more 855 favorable to the CPUs. But in spite of the debates about the 856 definitions of the speedup factor, a common consensus 857 among both the theoreticians and the practitioners is that 858 GPUs are relatively low-cost, low-power-consumption, 859 powerful co-processors that are suitable for SIMD-type 860 calculations and studies about efficient implementations of 861 numerical algorithms for scientific computing on the GPU 862 architectures are worthwhile. In this sense, the lessons learned through the implementation and optimization 863

process are more important than the exact speedup num-864 bers that we have obtained. 865

Unlike implementations on a single GPU, to port the 866 codes to multiple GPUs effectively, we need to deal with 867 an extra layer of complexity introduced by inter-process 868 communications. For the ADER-DG method, in which a 869 majority of the calculations are local to each element, we 870 can hide the inter-process communication overhead by 871 872 overlapping communication with computation. We separate the elements on a subdomain into inner and outer 873 elements. Once the computation on the outer elements is 874 completed, we can fill the MPI buffer using a separate 875 stream on the GPU and issue a non-blocking MPI call on 876 the CPU. While the MPI messages are traveling across the 877 878 network, the GPU proceeds to perform computations on the inner elements, and all other computations that do not need 879 information from the outer elements. The technologies for 880 multiple-GPU and CPU-GPU inter-connections are rapidly 881 evolving, and GPU-Aware MPI (GAMPI) libraries for 882 CUDA-enabled devices are gradually emerging. It is likely 883 that the process for overlapping communication with 884

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computation by taking advantage of the multiple-stream
capabilities of GPUs (i.e., task parallelism) will be much
simplified and become more efficient in the near future.

888 A sizeable portion of the speedup we obtained is owed 889 to the use of our customized matrix-matrix multiplication 890 kernels. In our implementation, the results of the multi-891 plications are evaluated analytically in terms of the non-892 zeros in the matrices whose locations can be determined 893 beforehand and are fixed throughout the program. This 894 approach allows us to condense the calculations by 895 exploiting the sparsity of the matrices and also gives us 896 enough freedom to manually adjust memory access patterns to minimize uncoalesced global memory accesses. 897 898 This approach is applicable because the matrices involved 899 in the ADER-DG method are element-local and relatively 900 small (e.g., for a 5th-order scheme the size of the stiffness 901 matrices is only 35 by 35), and the structures of these matrices are determined only by the specific forms of the 902 903 spatial basis functions used to approximate the solution in 904 the reference element. For more general matrix-matrix 905 multiplication problems, some off-the-shelf, pre-tuned 906 GPU linear algebra libraries, such as CUBLAS and cu-907 SPARSE, might be more suitable.

908 The work described in this article is vender-specific. But 909 we believe that most of the algorithmic analysis and 910 implementation ideas presented here can be reused either 911 identically or with slight modifications to adapt the ADER-912 DG method to other related architectures. To reinforce this 913 point, we note that the emerging OpenCL industry standard 914 for parallel programming of heterogeneous systems speci-915 fies a programming model that is very similar to CUDA. As 916 GPUs are being widely adopted as powerful and energy-917 efficient co-processors in modern-day computer clusters, 918 the work described here may help to accelerate the adop-919 tion of the ADER-DG method for seismic wave propaga-920 tion simulations on such heterogeneous clusters.

921 This work provides an accurate yet flexible forward 922 simulation solution other than conventional finite-differ-923 ence method. With the capability of unstructured mesh and 924 topography, our ADER-DG CUDA code could handle 925 some complex scenario along with a relatively high effi-926 ciency and accuracy. This work could be further applied to 927 earthquake related applications, such as full-wave seismic tomography (e.g., Chen et al. 2007; Liu and Tromp 2006; 928 929 Tromp et al. 2008), accurate earthquake source inversion 930 (e.g., Chen et al. 2005, 2010; Lee et al. 2011), seismic 931 hazard analysis (e.g., Graves et al. 2010), and reliable 932 ground-motion predictions (e.g., Graves et al. 2008; Ko-933 matitsch et al. 2004; Olsen 2000).

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