COP 5106 – Fall 2017 - Homework 1

Due: October 16, 2017

Instructions:

- Submit your answers in the form of a single document file
- Include the flow of the reasoning and calculations in the text.
- Remember that the homework is **individual** work.

Problem 1 (40 points):

Consider three different processors P1, P2 and P3, each having the same instruction set.

Processor	Clock rate	CPI	
P1	4.0 GHz	1.5	
P2	2.0 GHz	1.0	
P3	3.0 GHz	2.2	

a) Which processor has a highest performance expressed in instructions / second?

b) Each processor executes a program PR1, PR2 and PR3 respectively. It turns out that each program takes exactly 5 seconds to run on the respective processors. Find the number of instructions in the programs and the number of cycles it took each processor to execute them.

c) If we would execute programs PR1, PR2 and PR3 on processor P1, which one would take the longest?

d) Would the answer to c) change, if we would have asked about processor P2 or P3? In one sentence, explain why.

e) We are increasing the clock rate of the three processors, such that the program execution times decrease from 5 sec to 3 seconds. Unfortunately, the this requires architectural changes on each processor that increase the CPI on each processor with 20% respectively.
Calculate the new clock rates for each processors.

Problem 2 (40 points):

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes A, B, C and D based on their CPI.
We have two processors:

Processor	Clock rate (GHz)	CPI for instructions in in class A	CPI for instructions in in class B	CPI for instructions in in class C	CPI for instructions in in class D
P1	2.5	1	2	3	3
P2	3.0	2	2	2	2

Given a program with a dynamic instruction count of 10^6 instructions divided into classes as follows: 10% Class A, 20% Class B, 50% Class C, 20% Class D.

a) Which processor is faster: P1 or P2?

b) What is the global CPI for each implementation?

c) Find the clock cycles required in both cases.

Problem 3 (40 points):

Suppose that a processor with a load/store architecture executes at a clock rate of 2GHz, with the ideal CPI of 1.5. The typical applications run on this processor contain a mix of 60% arithmetic and logic instructions, 20% load and store instructions and 20% control instructions.

The processor accesses the memory through a separate data and instruction cache. An average 2% of the instructions produce an instruction miss, with a penalty of 25 clock cycles. An average of 12% of the data accesses are cache misses. The penalty of a data cache miss is 60 clock cycles. Cache hits do not produce any penalty (the memory access time of a cache hit is 1 cycle).

(a) What is the real CPI of the architecture?

(b) What is the average memory access time (AMAT) of the architecture?