# COP 5106 – Fall 2016 - Homework 1

Due: October 12, 2016

**Instructions:**

- Submit your answers in the form of a single document file
- Include the flow of the reasoning and calculations in the text.
- Remember that the homework is **individual** work.

**Problem 1:**

Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3GHz clock and CPI of 1.5. P2 has a 2.5GHz clock rate and a CPI of 1.0. P3 has a 4.0GHz clock rate and a CPI of 2.2.
a) Which processor has a highest performance expressed in instructions / second?
b) If the processors execute a program in 10 seconds, find the number of cycles and the number of instructions
c) We are trying to reduce the execution time by 30% but this leads to an increase of 20% of the CPI. What clock rate should we have to get this time reduction?

**Problem 2:**

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes A, B, C and D based on their CPI.
We have processors:

- P1 with clock rate 2.5GHz, CPIs 1,2,3,3
- P2 with clock rate 3.0GHz, CPIs 2,2,2,2

Given a program with a dynamic instruction count of 10E6 instructions divided into classes as follows: 10% Class A, 20% Class B, 50% Class C, 20% Class D.

a) Which is faster P1 or P2?
b) What is the global CPI for each implementation?
c) Find the clock cycles required in both cases.

**Problem 3:**

Suppose that a processor with a load/store architecture executes at a clock rate of 2GHz, with the ideal CPI of 1.5. The typical applications run on this processor contain a mix of 60% arithmetic and logic instructions, 20% load and store instructions and 20% control instructions.

The processor accesses the memory through a separate data and instruction cache. An average 2% of the instructions produce an instruction miss, with a penalty of 25 clock cycles. An average of 12% of the data

accesses are cache misses. The penalty of a data cache miss is 60 clock cycles. Cache hits do not produce any penalty.

(a) What is the real CPI of the architecture?
(b) What is the average memory access time (AMAT) of the architecture?