Operating Systems

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1

Consider a paging memory system with a TLB. How many I/O operations might be executed when there is a miss in the TLB?

2

Consider a paging system with the page table stored in memory.

2.1

If a memory reference takes 200 ns, how long does a paged memory reference take?

2.2

If we add associative registers, and 75 percent of all page-table references are found in the associative registers. What is the effective memory reference time? (Assume that finding a page-table entry in the associative memory takes zero time, if the entry is there.)

3

Suppose we have a memory with 32-bit virtual addresses and 4KB pages. If the page table is full (with 2^20 pages), show that a 20-level page table consumes approximately twice the space of a single level page table.

4

In a system with paging and segmentation, each virtual address (s,p,w) requires three memory accesses. To speed up the address translation, a translation look-aside buffer holds the components (s,p) together with the corresponding frame number. If each memory access takes m ns and the access to the TLB takes $m/10$ ns, determine the hit ratio necessary to reduce the average access time to memory by 50

5

Consider a system that uses both paging and segmentation. Use the following assumptions: 1. Virtual memory address size is 32 bits 2. s represents the number of bits needed for segments 3. p represents the number of bits needed for paging 4. Offset bits, $|w|$, are 10 bits.

5.1

Describe the difference between a paging system and a paging with segmentation like the one given above. Discuss their pros and cons.

5.2

What is the page size?

5.3

Assume that each entry in the page table takes one word and each page table is as big as a single page, what is $|p|$?

5.4

How many entries are there in a segment table?

6

At the system generation time you decide to have an address space of 1 GB.

6.1

What is the size of the swap area you need to allocate in this case?

6.2

Consider a paging system with a page size of 1 KB and a page table entry of 100 bytes. Assume that the page tables are resident and cannot be paged out. You have an application which needs 300 MB and allocates dynamically an array of 800 MB. Then the application searches sequentially through this array. How many page faults do you expect in the worst case? Draw the memory map for this case. Assume also that the resident requires an average of 100 pages that cannot be paged out.

6.3

Now assume that the paging tables are not resident and you have a TLB with 100 entries. Would the presence of the TLB decrease the number of page faults for this particular application?

7

Explain why it is easier to share a reentrant module using segmentation than it is to do so when pure paging is used.