Chapter 8: Input and Output
Chapter Contents

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8.2 Bridge-Based Bus Architectures
8.3 Communication Methodologies
8.4 Case Study: Communication on the Intel Pentium Architecture
8.5 Mass Storage
8.6 Input Devices
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Simple Bus Architecture

- A simplified motherboard of a personal computer (top view):
Simplified Illustration of a Bus

- Control ($C_0 - C_9$)
- Address ($A_0 - A_{31}$)
- Data ($D_0 - D_{31}$)
- Power (GND, +5V, -15V)
100 MHz Bus Clock

Crystal Oscillator

10 ns

Logical 0 (0V)
Logical 1 (+5V)
The Synchronous Bus

- Timing diagram for a synchronous memory read (adapted from [Tanenbaum, 1999]).
The Asynchronous Bus

- Timing diagram for asynchronous memory read (adapted from [Tanenbaum, 1999]).
Bus Arbitration

(a) Simple centralized bus arbitration; (b) centralized arbitration with priority levels; (c) decentralized bus arbitration. (Adapted from [Tanenbaum, 1999]).
Bridge Based Bus Architecture

- Bridging with dual Pentium II Xeon processors on Slot 2.

(Source: http://www.intel.com.)
Programmed I/O

Flowchart for a Disk Transfer

1. Enter
2. Check status of disk
   - No
     - Disk ready?
       - No
         - Send data from memory to disk (when writing) or from disk to memory (when reading).
       - Yes
         - Continue
3. Yes
   - Done?
     - No
       - Continue
     - Yes
Interrupt Driven I/O Flowchart for a Disk Transfer

1. Enter
2. Issue read or write request to disk.
3. Do other processing, until disk issues an interrupt.
   - Interrupt causes current processing to stop.
4. Transfer data between disk and memory.
   - Return from interrupt. Normal processing resumes.
5. Done?
   - No
   - Yes
6. Continue
DMA Transfer from Disk to Memory Bypasses the CPU
DMA Flowchart for a Disk Transfer

1. Enter

2. CPU sets up disk for DMA transfer

3. DMA device begins transfer independent of CPU

4. DMA device interrupts CPU when finished

5. CPU executes another process

6. Continue
Intel Memory and I/O Address Spaces

Address
00000000

Memory Space

Address
FFFF

I/O Space

Address
0000
Standard Intel Pentium Read and Write Bus Cycles
Intel Pentium Burst Read Bus Cycle

- **CLK**: T1, T2, T2, T2, T2, T2, Ti
- **ADDR**: Valid to Invalid
- **ADS#**:
- **CACHE#**:
- **W/R#**: Read
- **BRDY#**:
- **DATA**: TO CPU TO CPU TO CPU TO CPU
  - READ READ READ READ
Intel Pentium
Hold-Hold
Acknowledge
Bus Cycle
A Magnetic Disk with Three Platters

- Top surface not used
- Surface 3
- Surface 2
- Surface 1
- Surface 0
- Bottom surface not used
- Spindle
- Comb
- Read/write head (1 per surface)
- Direction of arm (comb) motion
- Head
- Air cushion
- Surface
- 5 μm
Manchester Encoding

- (a) Straight amplitude (NRZ) encoding of ASCII ‘F’; (b) Manchester encoding of ASCII ‘F’.

(a) Time

<table>
<thead>
<tr>
<th>Voltage</th>
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<tbody>
<tr>
<td>1 0 0 0 0 1 1 0</td>
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</tbody>
</table>

= ‘F’

Time

(b) Time

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<td>1 0 0 0 0 1 1 0</td>
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</table>

= ‘F’

Time
Organization of a Disk Platter with a 1:2 Interleave Factor
### Master Control Block

- **No. surfaces on disk = 4**
- **No. tracks/surface = 814**
- **No. sectors/track = 32**
- **No. bytes/sector = 512**
- **Interleave factor = 1:3**

#### Starting sector, or sector list

<table>
<thead>
<tr>
<th>Filename</th>
<th>Surface</th>
<th>Track</th>
<th>Sector</th>
<th>Creation Date</th>
<th>Last Modified</th>
<th>Owner</th>
<th>Protections</th>
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<tbody>
<tr>
<td>xyz.p</td>
<td>1</td>
<td>10</td>
<td>5</td>
<td>11/14/93</td>
<td>11/14/93</td>
<td>16</td>
<td>RWX by Owner</td>
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<tr>
<td></td>
<td>1</td>
<td>12</td>
<td>7</td>
<td>10:30:57</td>
<td>19:30:57</td>
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<td>2</td>
<td>23</td>
<td>4</td>
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<tr>
<td>ab.c</td>
<td>1</td>
<td>10</td>
<td>8</td>
<td>8/18/93</td>
<td>1/21/94</td>
<td>20</td>
<td>RX - All W-Owner</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>95</td>
<td>2</td>
<td>16:03:12</td>
<td>14:45:03</td>
<td></td>
<td>R = Read W = Write X = Execute</td>
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<td>2</td>
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#### Files

- **Free blocks**
  - 1 1 0
  - 1 1 1
  - 1 2 5
  - ...

- **Bad blocks**
  - 1 1 3
  - 2 5 7
  - ...

---

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Magnetic Tape

- A portion of a magnetic tape (adapted from [Hamacher, 1990]).
Magnetic Drum

Fixed read/write heads (1 per track)

Sector

Tracks
Spiral Format for Compact Disk
**ECMA-23 Keyboard Layout**

- Keyboard layout for the ECMA-23 Standard (2nd ed.). Shift keys are frequently placed in the B row.

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The Dvorak Keyboard Layout

Bit Pad with Puck

Cable to host computer

Puck

Coil

Buttons
Mouse and Trackball

- A three-button mouse (left) and a three-button trackball (right).
Lightpen

- A user selects an object with a lightpen.
**Touchscreen**

- A user selects an object on a touchscreen.

![Touchscreen Diagram]

- **LEDs (sources)**
- **Detector**
- **User breaks beams**
Joystick

- A joystick with a selection button and a rotatable rod:
Laser Printer

- Schematic of a laser printer (adapted from [Tanenbaum, 1999]).

Page description from host computer → Page composing circuitry

Stationary laser source → Rotating mirror

Charged pattern

Toner cartridge

Cleaner and discharger

Heated rollers

Paper input → Paper output
Cathode Ray Tube

- A CRT with a single electron gun:

  - Electron gun
  - Horizontal control
  - Vertical control
  - Intensity control
  - Vertical deflection plate
  - Horizontal deflection plate
  - Grid
  - Vacuum
  - Phosphor coated screen
Display Controller

- Display controller for a 640×480 color monitor (adapted from [Hamacher et al., 1990]).

Clock → Column counter (mod 640) → Row counter (mod 480)

To horizontal deflection plate control

One output pulse per 640 columns

To vertical deflection plate control

Address

LUT loaded from computer

Screen image loaded by computer

RAM

Frame buffer

Address

Output

Input

To electron gun (grid) control

Red

Green

Blue

8

8

8

RAM

LUT