Principles of Computer Architecture

Miles Murdocca and Vincent Heuring

Chapter 3: Arithmetic

Principles of Computer Architecture by M. Murdocca and V. Heuring

3-1

Chapter Contents

3.1 Overview

3.2 Fixed Point Addition and Subtraction

3.3 Fixed Point Multiplication and Division

3.4 Floating Point Arithmetic

3.5 High Performance Arithmetic

3.6 Case Study: Calculator Arithmetic Using Binary Coded Decimal

Computer Arithmetic

- Using number representations from Chapter 2, we will explore four basic arithmetic operations: addition, subtraction, multiplication, division.
- Significant issues include: fixed point vs. floating point arithmetic, overflow and underflow, handling of signed numbers, and performance.
- We look first at fixed point arithmetic, and then at floating point arithmetic.

Number Circle for 3-Bit Two's Complement Numbers

- Numbers can be added or subtracted by traversing the number circle clockwise for addition and counterclockwise for subtraction.
- Overflow occurs when a transition is made from +3 to -4 while proceeding around the number circle when adding, or from -4 to +3 while subtracting.



Overflow

- Overflow occurs when adding two positive numbers produces a negative result, or when adding two negative numbers produces a positive result. Adding operands of unlike signs never produces an overflow.
- Notice that discarding the carry out of the most significant bit during two's complement addition is a normal occurrence, and does not by itself indicate overflow.
- As an example of overflow, consider adding $(80 + 80 = 160)_{10}$, which produces a result of -96_{10} in an 8-bit two's complement format:
 - 01010000 = 80
 - + 01010000 = 80

10100000 = -96 (not 160 because the sign bit is 1.)

Principles of Computer Architecture by M. Murdocca and V. Heuring

Ripple Carry Adder

• Two binary numbers A and B are added from right to left, creating a sum and a carry at the outputs of each full adder for each bit position.



Principles of Computer Architecture by M. Murdocca and V. Heuring

Constructing Larger Adders

• A 16-bit adder can be made up of a cascade of four 4-bit ripplecarry adders.



Principles of Computer Architecture by M. Murdocca and V. Heuring

© 1999 M. Murdocca and V. Heuring

Full Subtractor

• Truth table and schematic symbol for a ripple-borrow subtractor:

a_i	b _i	<i>bor_i</i>	<i>diff_i</i>	bor _{i+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Ripple-Borrow Subtractor

- A ripple-borrow subtractor can be composed of a cascade of full subtractors.
- Two binary numbers A and B are subtracted from right to left, creating a difference and a borrow at the outputs of each full subtractor for each bit position.



Principles of Computer Architecture by M. Murdocca and V. Heuring

Chapter 3: Arithmetic

Combined Adder/Subtractor

• A single ripple-carry adder can perform both addition and subtraction, by forming the two's complement negative for B when subtracting. (Note that +1 is added at c_0 for two's complement.)



One's Complement Addition

 An example of one's complement integer addition with an endaround carry:



 $0\ 0\ 0\ 0\ 1\ (+1)_{10}$

• The end-around carry is needed because there are two representations for 0 in one's complement. Both representations for 0 are visited when one or both operands are negative.

Principles of Computer Architecture by M. Murdocca and V. Heuring

Number Circle (Revisited)

• Number circle for a three-bit signed one's complement representation. Notice the two representations for 0.



End-Around Carry for Fractions

- The end-around carry complicates one's complement addition for non-integers, and is generally not used for this situation.
- The issue is that the distance between the two representations of 0 is 1.0, whereas the rightmost fraction position is less than 1.

Principles of Computer Architecture by M. Murdocca and V. Heuring

Multiplication Example

 Multiplication of two 4-bit unsigned binary integers produces an 8-bit result.

			1	1	0	1	$(13)_{10}$ Multiplicand M
		\times	1	0	1	1	(11) ₁₀ Multiplier Q
			1	1	0	1	
		1	1	0	1		Partial products
	0	0	0	0			i artiai productis
1	1	0	1				
0	0	0	1	1	1	1	$(143)_{10}$ Product P

• Multiplication of two 4-bit signed binary integers produces only a 7-bit result (each operand reduces to a sign bit and a 3-bit magnitude for each operand, producing a sign-bit and a 6-bit result).

Principles of Computer Architecture by M. Murdocca and V. Heuring

A Serial Multiplier



Example of Multiplication Using Serial Multiplier



Example of Base 2 Division

• $(7 / 3 = 2)_{10}$ with a remainder R of 1.

3-17

• Equivalently, $(0111/11 = 10)_2$ with a remainder R of 1.

Principles of Computer Architecture by M. Murdocca and V. Heuring

Serial Divider



Principles of Computer Architecture by M. Murdocca and V. Heuring

3-19 Chapter 3: Arithmetic Division Example Using Serial Divider



Principles of Computer Architecture by M. Murdocca and V. Heuring

Multiplication of Signed Integers

- Sign extension to the target word size is needed for the negative operand(s).
- A target word size of 8 bits is used here for two 4-bit signed operands, but only a 7-bit target word size is needed for the result.



Carry-Lookahead Addition

$$s_{i} = \overline{a_{i}b_{i}c_{i}} + \overline{a_{i}b_{i}c_{i}} + a_{i}\overline{b_{i}c_{i}} + a_{i}b_{i}c_{i}$$

$$c_{i+1} = b_{i}c_{i} + a_{i}c_{i} + a_{i}b_{i}$$

$$c_{i+1} = a_{i}b_{i} + (a_{i} + b_{i})c_{i}$$

$$c_{i+1} = G_{i} + P_{i}c_{i}$$

$$e^{\mathbf{v}}$$

 Carries are represented in terms of G_i (generate) and P_i (propagate) expressions.

$$G_{i} = a_{i}b_{i} \text{ and } P_{i} = a_{i} + b_{i}$$

$$c_{0} = 0$$

$$c_{1} = G_{0}$$

$$c_{2} = G_{1} + P_{1}G_{0}$$

$$c_{3} = G_{2} + P_{2}G_{1} + P_{2}P_{1}G_{0}$$

$$c_{4} = G_{3} + P_{3}G_{2} + P_{3}P_{2}G_{1} + P_{3}P_{2}P_{1}G_{0}$$

Principles of Computer Architecture by M. Murdocca and V. Heuring

© 1999 M. Murdocca and V. Heuring

Chapter 3: Arithmetic

Carry Lookahead Adder



 Maximum gate delay for the carry generation is only 3. The full adders introduce two more gate delays. Worst case path is 5 gate delays.

Principles of Computer Architecture by M. Murdocca and V. Heuring

3-22

Floating Point Arithmetic

- Floating point arithmetic differs from integer arithmetic in that exponents must be handled as well as the magnitudes of the operands.
- The exponents of the operands must be made equal for addition and subtraction. The fractions are then added or subtracted as appropriate, and the result is normalized.
- Ex: Perform the floating point operation: $(.101 \times 2^3 + .111 \times 2^4)_2$
- Start by adjusting the *smaller* exponent to be equal to the larger exponent, and adjust the fraction accordingly. Thus we have .101 $\times 2^3 = .010 \times 2^4$, losing .001 $\times 2^3$ of precision in the process.
- The resulting sum is (.010 + .111) \times 2⁴ = 1.001 \times 2⁴ = .1001 \times 2⁵, and rounding to three significant digits, .100 \times 2⁵, and we have lost another 0.001 \times 2⁴ in the rounding process.

Principles of Computer Architecture by M. Murdocca and V. Heuring

Floating Point Multiplication/Division

- Floating point multiplication/division are performed in a manner similar to floating point addition/subtraction, except that the sign, exponent, and fraction of the result can be computed separately.
- Like/unlike signs produce positive/negative results, respectively. Exponent of result is obtained by adding exponents for multiplication, or by subtracting exponents for division. Fractions are multiplied or divided according to the operation, and then normalized.
- Ex: Perform the floating point operation: (+.110 \times 2⁵) / (+.100 \times 2⁴)₂
- The source operand signs are the same, which means that the result will have a positive sign. We subtract exponents for division, and so the exponent of the result is 5 - 4 = 1.
- We divide fractions, producing the result: 110/100 = 1.10.
- Putting it all together, the result of dividing (+.110 \times 2⁵) by (+.100 \times 2⁴) produces (+1.10 \times 2¹). After normalization, the final result is (+.110 \times 2²).

The Booth Algorithm

- Booth multiplication reduces the number of additions for intermediate results, but can sometimes make it worse as we will see.
- Positive and negative numbers treated alike.



Principles of Computer Architecture by M. Murdocca and V. Heuring

A Worst Case Booth Example

 A worst case situation in which the simple Booth algorithm requires twice as many additions as serial multiplication.



Principles of Computer Architecture by M. Murdocca and V. Heuring

Bit-Pair Recoding (Modified Booth Algorithm)



3-27

Coding of Bit Pairs

Booth pai $(i + 1, i)$	r Recoded bit pair (<i>i</i>)	Corresponding multiplier bits (i + 1, i, i - 1)	
0 0	= 0	000 or 111	
0 +1	= +1	001	
0 -1	= -1	110	
+1 0	= +2	011	
+1 +1	= —		
+1 -1	= +1	010	
-1 0	= -2	100	
-1 +1	= -1	101	
-1 -1	= —		

Principles of Computer Architecture by M. Murdocca and V. Heuring

Parallel Pipelined Array Multiplier

3-29



Principles of Computer Architecture by M. Murdocca and V. Heuring

Newton's Iteration for Zero Finding

- The goal is to find where the function f(x) crosses the x axis by starting with a guess x_i and then using the error between f(x_i) and zero to refine the guess.
- A three-bit lookup table for computing *x*₀:

B = First three bits of b	Actual base 10 value of 1/B	Corresponding lookup table entry	
.100	2	10	
.101	1 3/5	01	
.110	1 1/3	01	
.111	1 1/7	01	

Principles of Computer Architecture by M. Murdocca and V. Heuring



 The division operation a/b is computed as a × 1/b. Newton's iteration provides a fast method of computing 1/b.

© 1999 M. Murdocca and V. Heuring

Residue Arithmetic

- Implements carryless arithmetic (thus fast!), but comparisons are difficult without converting to a weighted position code.
- Representation of the first twenty decimal integers in the residue number system for the given moduli:

Decimal	Residue 5794	Decimal	Residue 5794
0	0000	10	0312
1	1111	11	1423
2	2222	12	2530
3	3333	13	3641
4	4440	14	4052
5	0551	15	0163
6	1662	16	1270
7	2073	17	2381
8	3180	18	3402
9	4201	19	4513

Principles of Computer Architecture by M. Murdocca and V. Heuring

Examples of Addition and Multiplication in the Residue Number System

29 + 27 = 56				
Decimal	Residue 5794			
29 27 56	4121 2603 1020			

$10 \times 17 = 170$				
Decimal	Residue 5794			
10 17 170	0312 2381 0282			

Principles of Computer Architecture by M. Murdocca and V. Heuring

16-bit Group Carry Lookahead Adder

• A16-bit GCLA is composed of four 4-bit CLAs, with additional logic that generates the carries between the four-bit groups.

$$\begin{aligned} & GG_0 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 \\ & GP_0 = P_3P_2P_1P_0 \\ & c_4 = GG_0 + GP_0c_0 \\ & c_8 = GG_1 + GP_1c_4 = GG_1 + GP_1GG_0 + GP_1GP_0c_0 \\ & c_{12} = GG_2 + GP_2c_8 = GG_2 + GP_2GG_1 + GP_2GP_1GG_0 + \\ & GP_2GP_1GP_0c_0 \\ & c_{16} = GG_3 + GP_3c_{12} = GG_3 + GP_3GG_2 + GP_3GP_2GG_1 + \\ & GP_3GP_2GP_1GG_0 + GP_3GP_2GP_1GP_0c_0 \end{aligned}$$

Principles of Computer Architecture by M. Murdocca and V. Heuring

3-34 **Chapter 3: Arithmetic 16-Bit Group Carry Lookahead Adder** $a_8 - a_{11}$ $a_{12} - a_{15}$ $a_4 - a_7$ $a_0 - a_3$ $b_{12} - b_{15}$ $b_8 - b_{11}$ $b_4 - b_7$ $b_0 - b_3$ c_0 c_{12} C_8 C_{Λ} • Each CLA CLA_3 CLA_2 CLA_1 CLA_0 has a longest path of 5 gate de $s_8 - s_{11}$ $s_{12} - s_{15}$ $s_4 - s_7$ $S_0 - S_3$ lays. GP_3 GP_{2} GP_1 GP_0 GG_2 GG_2 GG_1 GG_0 Group Carry Lookahead Logic

• In the GCLL section, GG and GP signals are generated in 3 gate delays; carry signals are generated in 2 more gate delays, resulting in 5 gate delays to generate the carry out of each GCLA group and 10 gates delays on the worst case path (which is s_{15} – not c_{16}).

Principles of Computer Architecture by M. Murdocca and V. Heuring

HP 9100 Series Desktop Calculator

- Source: http://www.teleport.com/ ~dgh/91003q.jpg.
- Uses binary coded decimal (BCD) arithmetic.



Addition Example Using BCD

- Addition is performed digit by digit (*not* bit by bit), in 4-bit groups, from right to left.
- Example $(255 + 63 = 318)_{10}$:

3-36



Principles of Computer Architecture by M. Murdocca and V. Heuring

Subtraction Example Using BCD

- Subtraction is carried out by adding the ten's complement negative of the subtrahend to the minuend.
- Ten's complement negative of subtrahend is obtained by adding 1 to the nine's complement negative of the subtrahend.
- Consider performing the subtraction operation (255 63 = $192)_{10}$:



Principles of Computer Architecture by M. Murdocca and V. Heuring

Excess 3 Encoding of BCD Digits

 Using an excess 3 encoding for each BCD digit, the leftmost bit indicates the sign.

3-38

	BCD Bit Pattern	Normal BCD value	Excess 3 value	
	0 0 0 0	0	d	
	0 0 0 1	1	d	
	0 0 1 0	2	d	
	0 0 1 1	3	0	
, ost	0 1 0 0	4	1	Desitive
	0 1 0 1	5	2	numbers
	0 1 1 0	6	3	numbers
	0 1 1 1	7	4	
	1 0 0 0	8	5	
	1 0 0 1	9	6	Negative
	1 0 1 0	d	7	numbers
	1 0 1 1	d	8	
	1 1 0 0	d	9	
	1 1 0 1	d	d	
	1 1 1 0	d	d	
	1 1 1 1	d	d	
				1

Principles of Computer Architecture by M. Murdocca and V. Heuring

Chapter 3: Arithmetic

A BCD Full Adder

 Circuit adds two base 10 digits represented in **BCD.** Adding 5 and 7 (0101 and 0111) results in 12 (0010 with a carry of 1, and not 1100, which is the binary representation of 12_{10}).



Principles of Computer Architecture by M. Murdocca and V. Heuring

© 1999 M. Murdocca and V. Heuring

Ten's Complement Subtraction

Compare: the traditional signed magnitude approach for adding decimal numbers vs. the ten's complement approach, for (21 - 34 = -13)₁₀:



Principles of Computer Architecture by M. Murdocca and V. Heuring

© 1999 M. Murdocca and V. Heuring

BCD Floating Point Representation

 Consider a base 10 floating point representation with a two digit signed magnitude exponent and an eight digit signed magnitude fraction. On a calculator, a sample entry might look like:

```
\textbf{-.37100000} \times \textbf{10}^{\textbf{-12}}
```

- We use a ten's complement representation for the exponent, and a base 10 signed magnitude representation for the fraction. A separate sign bit is maintained for the fraction, so that each digit can take on any of the 10 values 0–9 (except for the first digit, which cannot be zero). We should also represent the exponent in excess 50 (placing the representation for 0 in the middle of the exponents, which range from -50 to +49) to make comparisons easier.
- The example above now looks like this (see next slide):

BCD Floating Point Arithmetic

• The example in the previous slide looks like this:

Sign bit: 1

Exponent: 0110 1011

- Note that the representation is still in excess 3 binary form, with a two digit excess 50 exponent.
- To add two numbers in this representation, as for a base 2 floating point representation, we start by adjusting the exponent and fraction of the smaller operand until the exponents of both operands are the same. After adjusting the smaller fraction, we convert either or both operands from signed magnitude to ten's complement according to whether we are adding or subtracting, and whether the operands are positive or negative, and then perform the addition or subtraction operation.

Principles of Computer Architecture by M. Murdocca and V. Heuring