CDA 5106 - Advanced Computer Architecture

Homework 2 (50 pts)

For all questions, use the following code and latencies (same as in HW2):

```
Loop: LD     F2,0(Rx)
I0:   DIVD   F8,F2,F0
I1:   MULTD  F2,F6,F2
I2:   LD     F4,0(Ry)
I3:   ADDD   F4,F0,F4
I4:   ADDD   F10,F8,F2
I5:   ADDI   Rx,Rx,#8
I6:   ADDI   Ry,Ry,#8
I7:   SD     F4,0(Ry)
I8:   SUB    R20,R4,Rx
I9:   BNZ    R20,Loop
```

Latencies beyond single cycle	
Memory LD	+4
Memory SD	+1
Integer ADD, SUB	+0
Branches	+1
ADDD	+1
MULTD	+5
DIVD	+12

Q1. (25 pts)

Unroll the loop twice in the above example and schedule the code for optimal execution (ignore structural hazards for now). Show your work. *Hint:* Make sure to take care of integer ops (ADDI etc). Use register renaming for all FP registers affected.

Q2. (25 pts)

Use the result from Q1. Assume you have the following hardware resources limited – only one LOAD/STORE unit and two FP Multiply units. All other resources are unlimited. Reschedule the code optimally to avoid the resulting structural hazards.