Lecture 1: Flynn's Taxonomy

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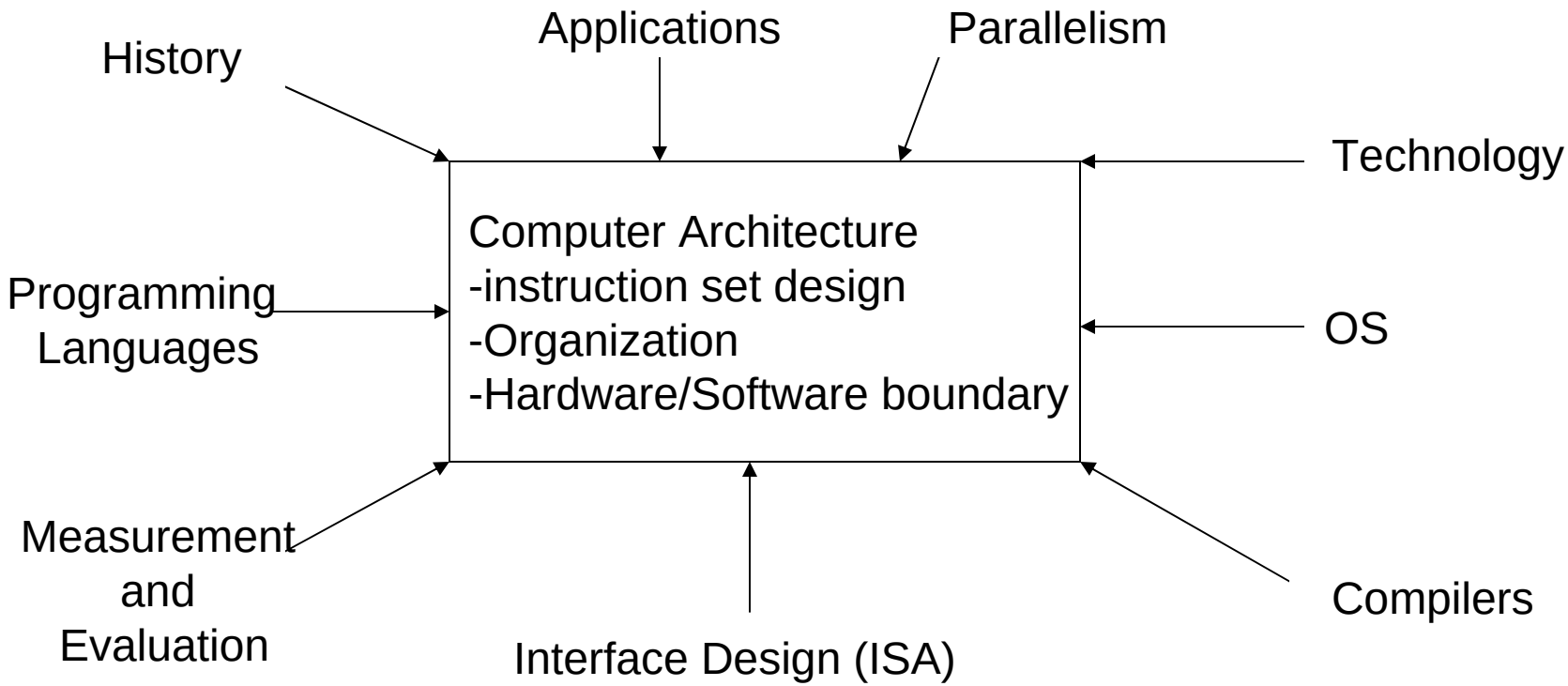
The Global View of Computer Architecture



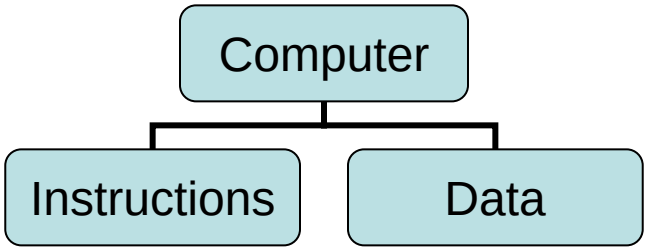
The Task of A Computer Designer

– Determine what attributes are important for a new machine.

– Design a machine to maximize performance while staying within cost constrains.

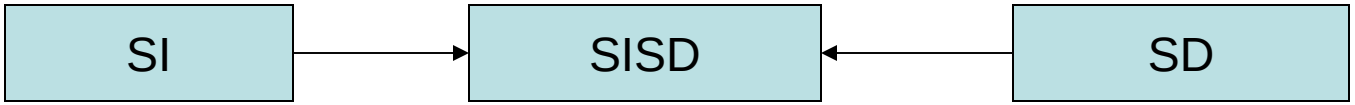
Flynn's Taxonomy

- Michael Flynn (from Stanford)
  - Made a characterization of computer systems which became known as Flynn's Taxonomy



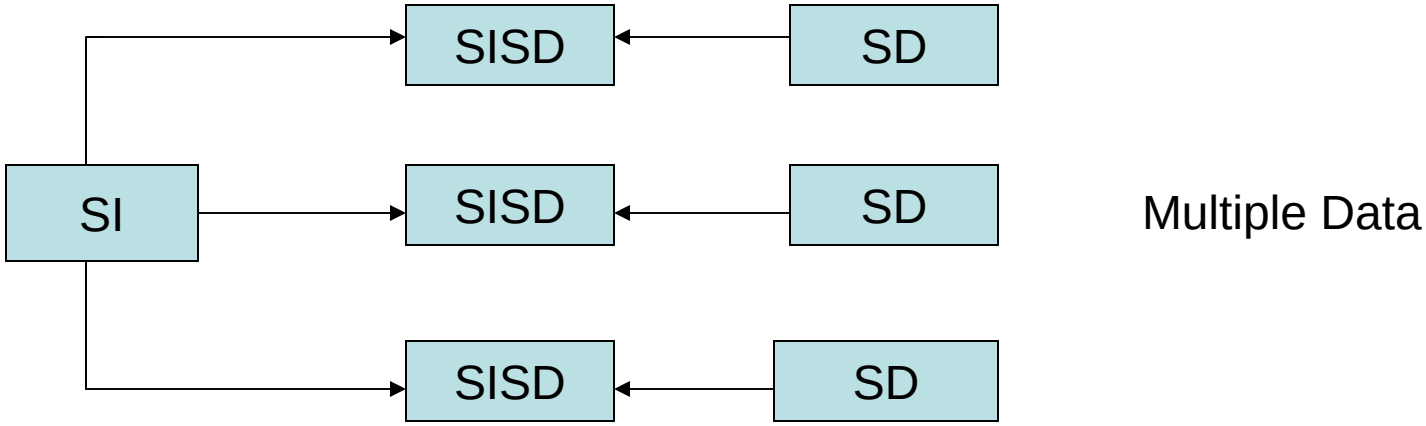
Flynn's Taxonomy

- SISD – Single Instruction Single Data Systems



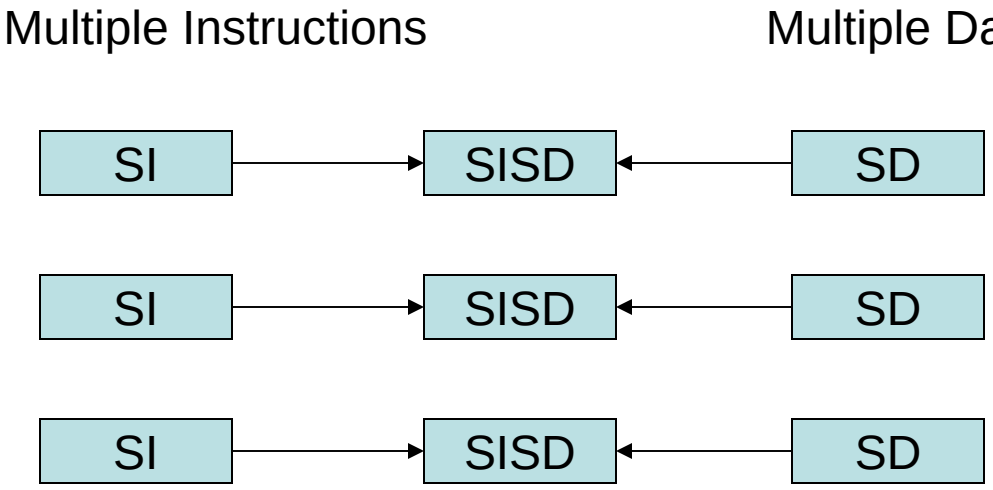
Flynn's Taxonomy

- SIMD – Single Instruction Multiple Data Systems "Array Processors"



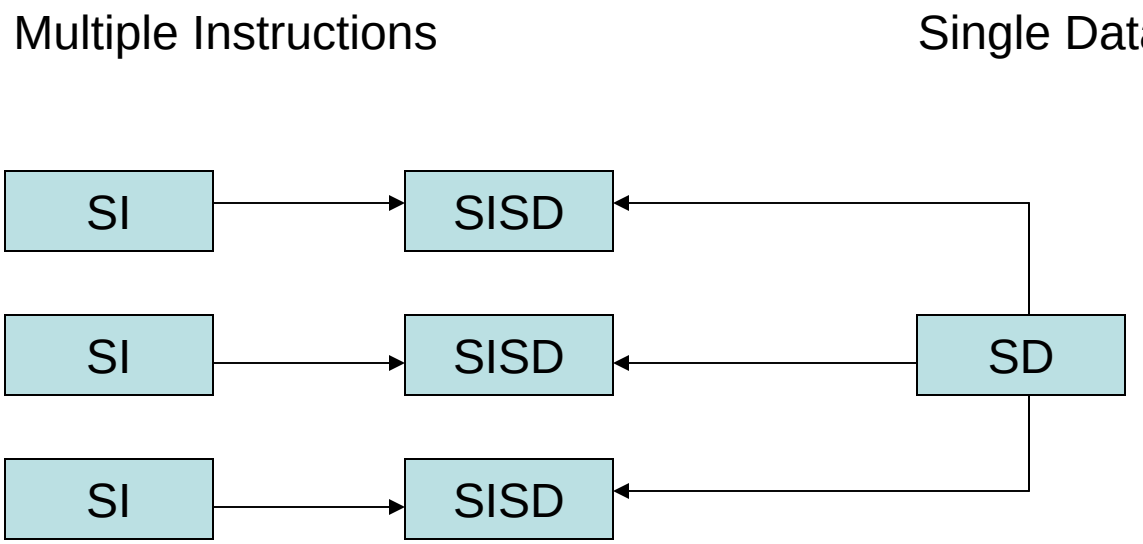
Flynn's Taxonomy

- MIMD Multiple Instructions Multiple Data System: "Multiprocessors"



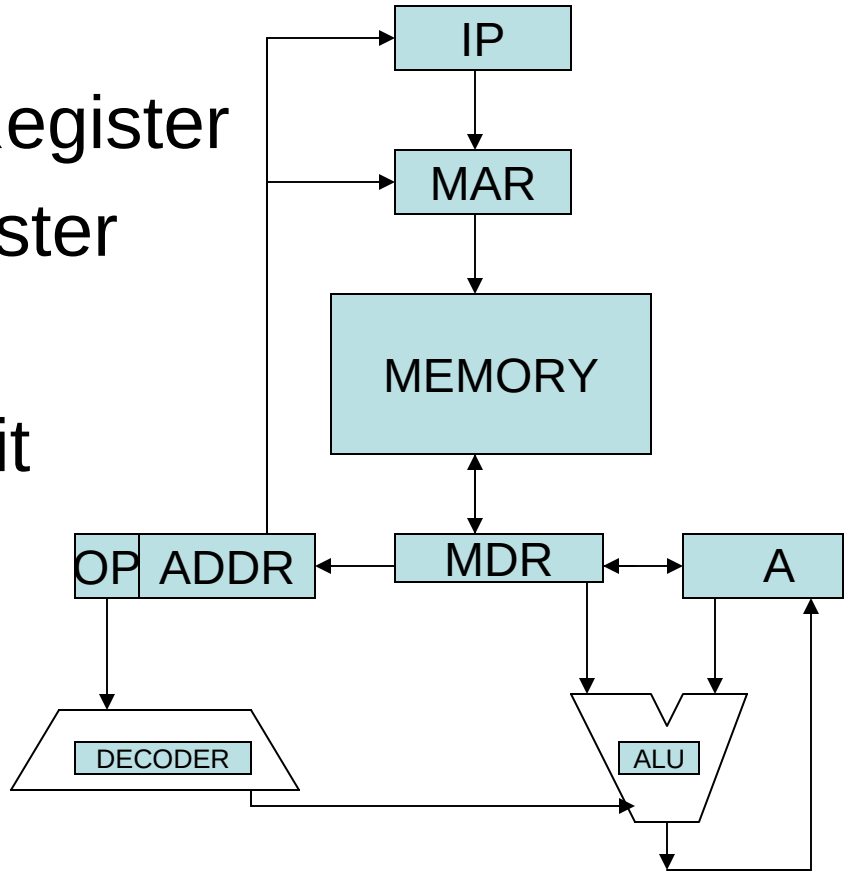
Flynn's Taxonomy

- MISD- Multiple Instructions / Single Data System
  - Some people say "pipelining" lies here, but this is debatable.



Abbreviations: SISD one address Machine.

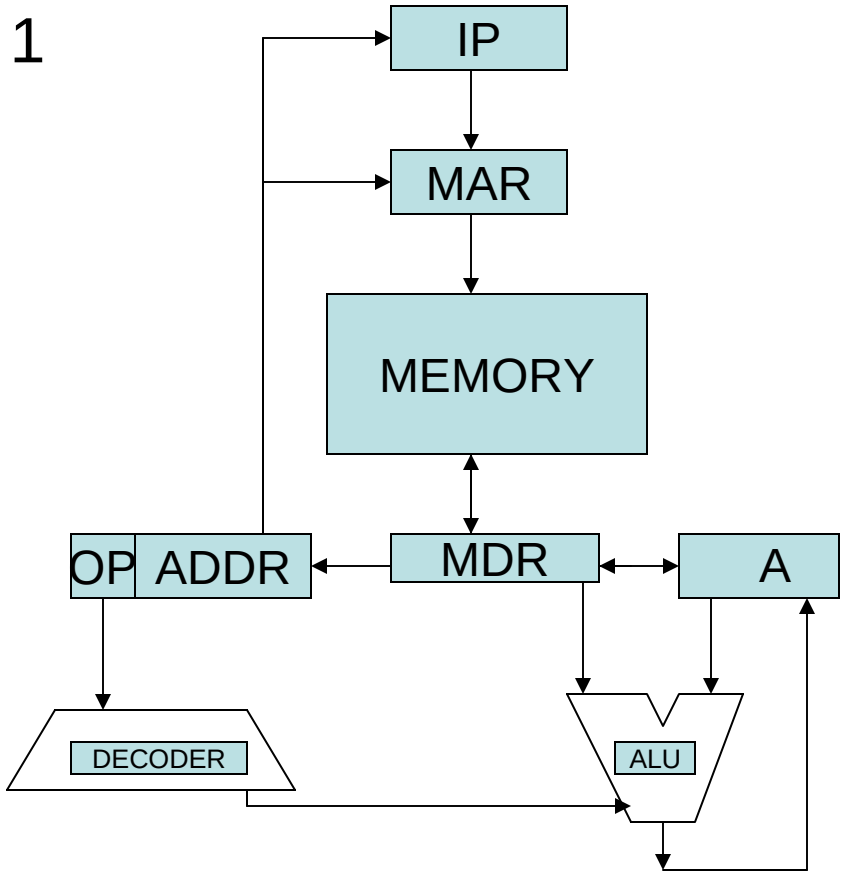
- IP: Instruction pointer
- MAR: Memory Address Register
- MDR: Memory Data Register
- A: Accumulator
- ALU: Arithmetic Logic Unit
- IR: Instruction Register
- OP: Opcode
- ADDR: Address



LOAD X

- MAR ← IP
- MDR ← M[MAR] || IP ← IP + 1
- IR ← MDR
- DECODER ←IR.OP
- MAR ← IR.ADDR
- MDR ←M[MAR]
- A ← MDR

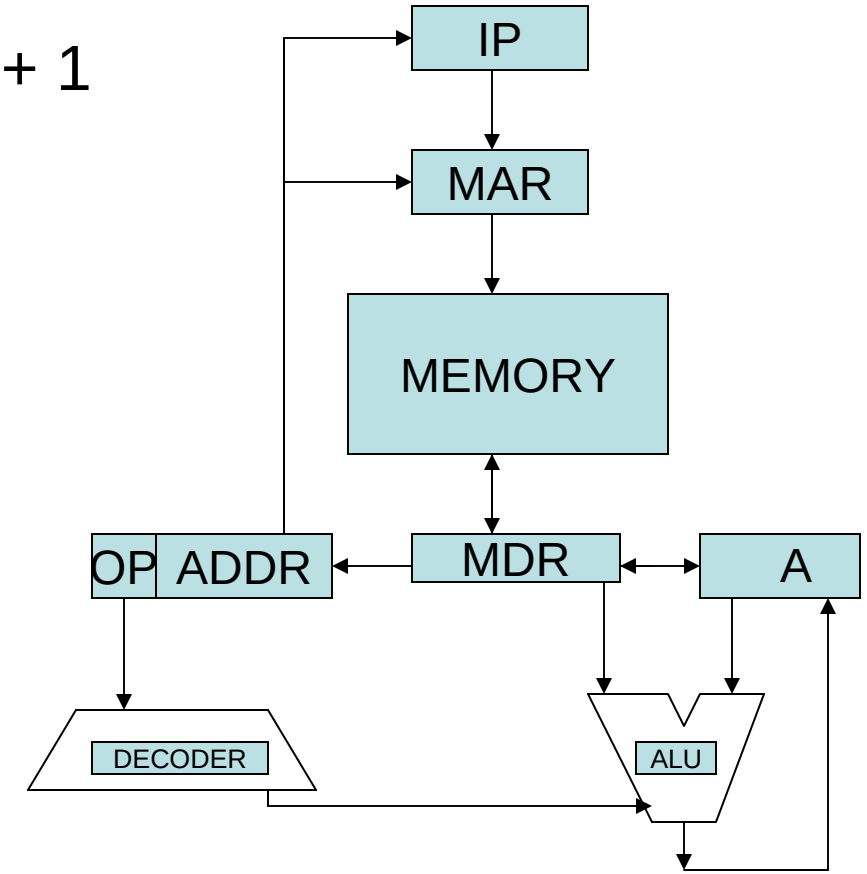
One address format



One address format

ADD X

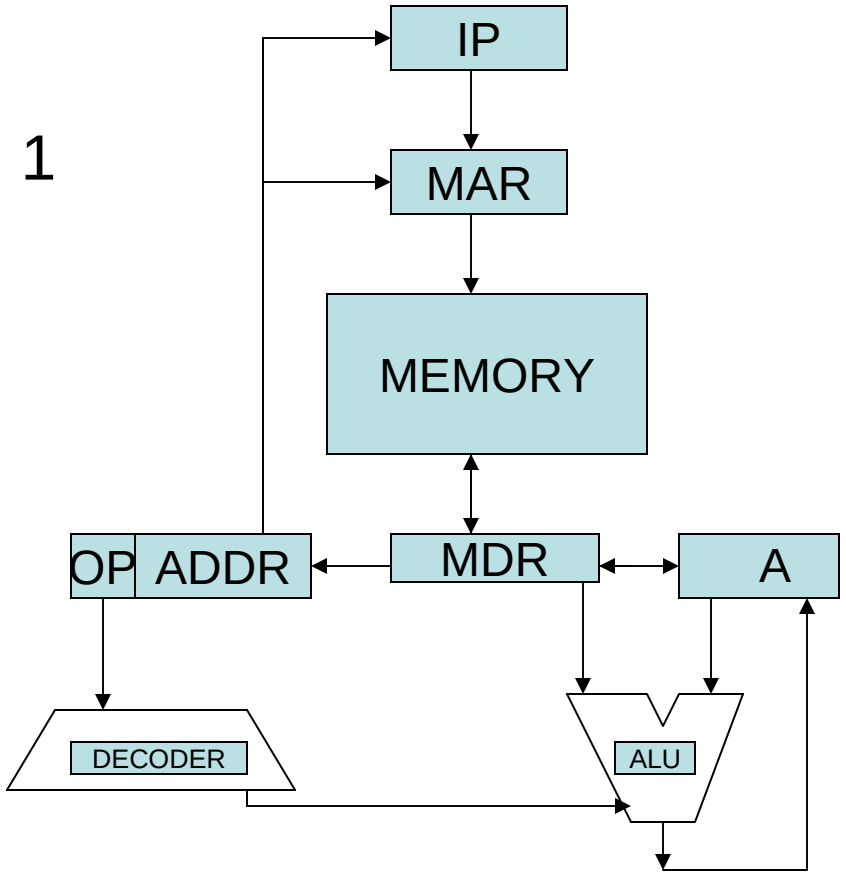
- MAR ← IP
- MDR ← M[MAR] || IP ← IP + 1
- IR ← MDR
- DECODER ←IR.OP
- MAR ← IR.ADDR
- MDR ←M[MAR]
- A ← A + MDR



STORE X

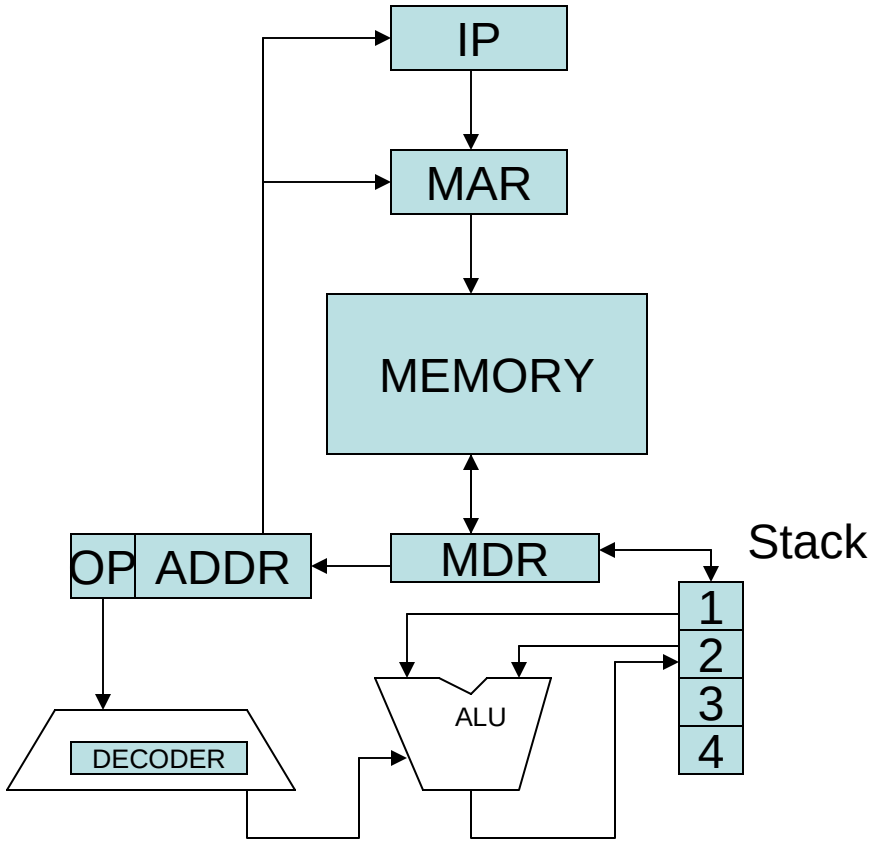
- MAR ← IP
- MDR ← M[MAR] || IP ← IP + 1
- IR ← MDR
- DECODER ←IR.OP
- MAR ← IR.ADDR
- MDR ← A
- M[MAR] ← MDR

One address format



SISD Stack Machine

- First Stack Machine
- B5000



PUSH

? ← ST[4] ||

ST[4] ← ST[3] ||

ST[3] ← ST[2] ||

ST[2] ← ST[1] ||

ST[1] ← MDR ||

"||" means in parallel

LOAD X

MAR ← IP

MDR ← M[MAR] || IP ← IP + 1

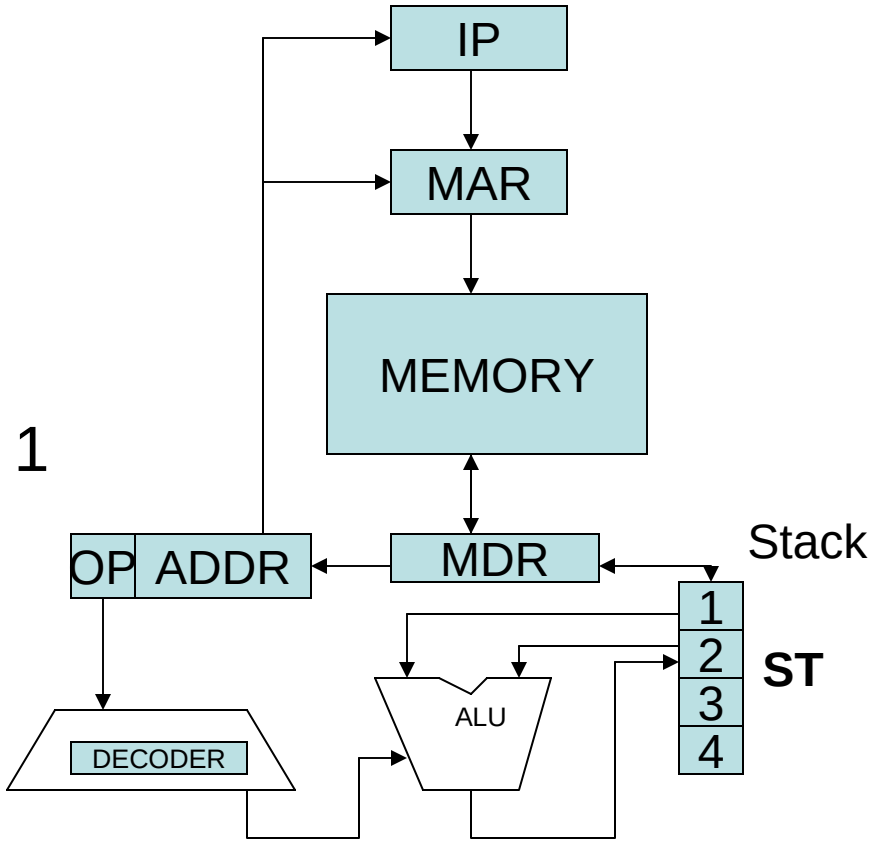
IR ← MDR

DECODER ←IR.OP

MAR ← IR.ADDR

MDR ←M[MAR]

PUSH



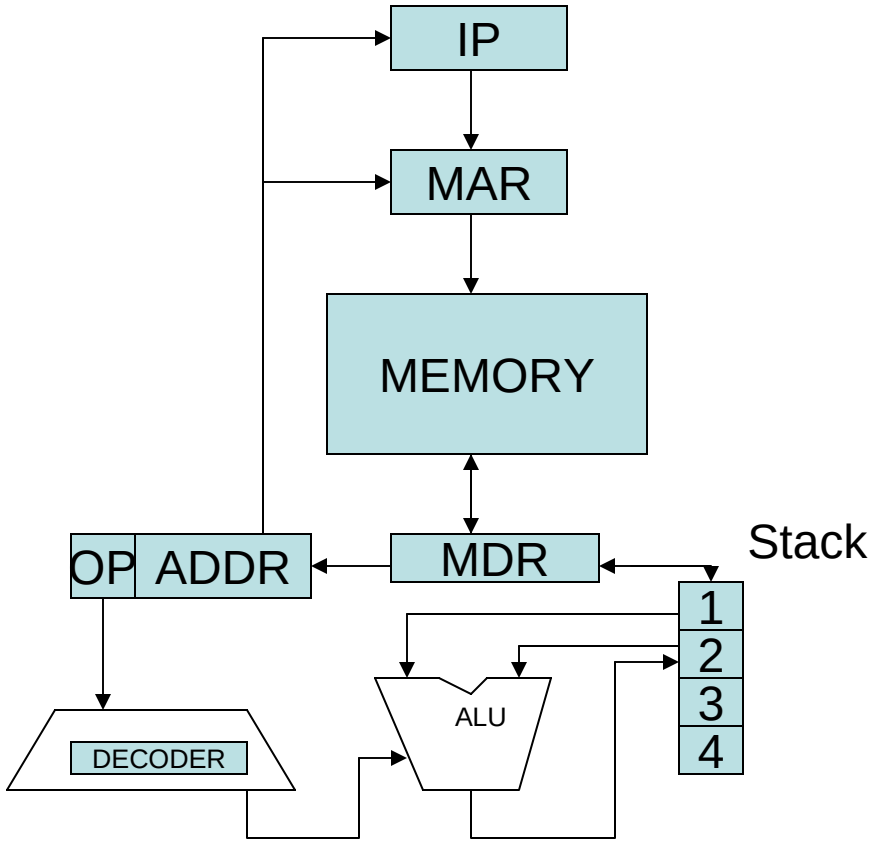
POP

MDR ←ST[1] ||
ST[1] ←ST[2] ||
ST[2] ←ST[3] ||
ST[3] ←ST[4] ||
ST[4] ← 0

STORE X

MAR ← IP
MDR ← M[MAR]
IR ← MDR
DECODER ← IR.OP
MAR← IR.ADDR
POP
M[MAR] ← MDR

"||" means in parallel

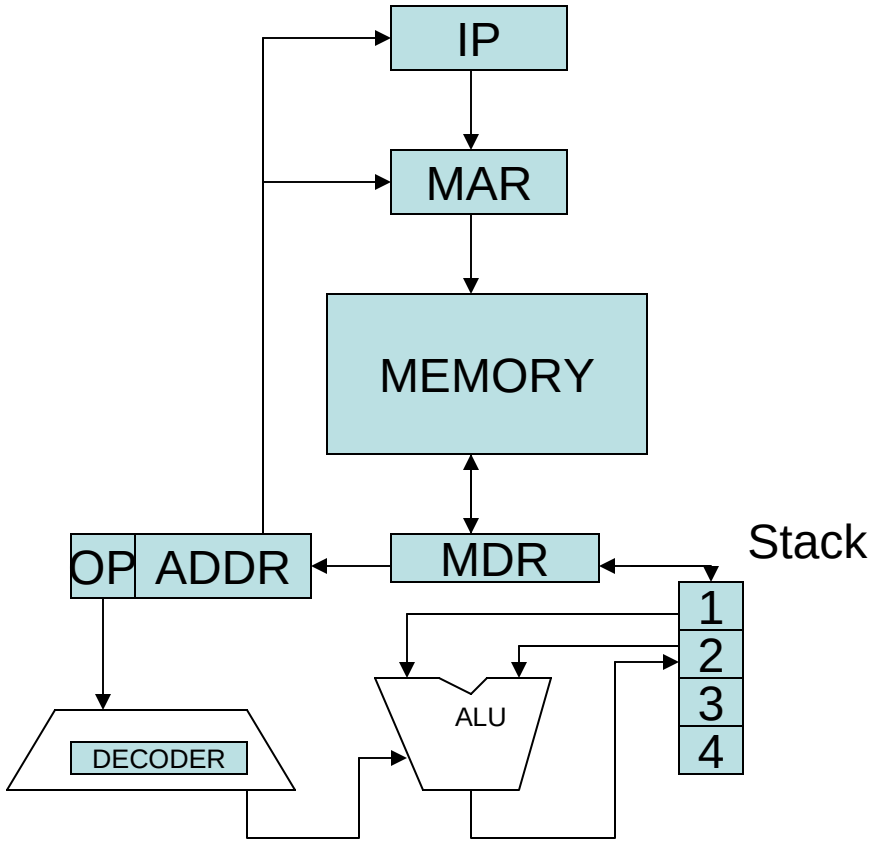


Zero address format

OP	NOT USED

ADD

MAR ← IP
MDR ← M[MAR]
IR ← MDR
DECODER ← IR.OP
ST[2] ← ST[1] + ST[2]
ST[1] ←ST[2]
ST[2] ←ST[3]
ST[3] ←ST[4]
ST[4] ← 0



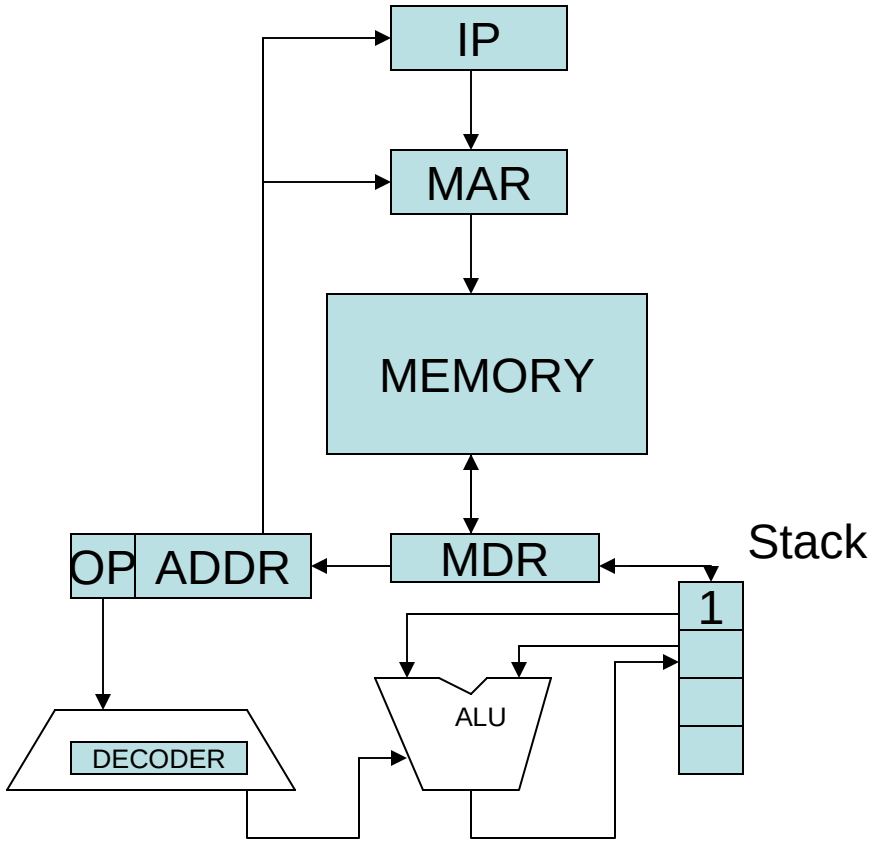
Example

- Stack Trace
  - Loadi 1 _ _ _ _
  - Loadi 2
  - Add
  - Store X

Cont’

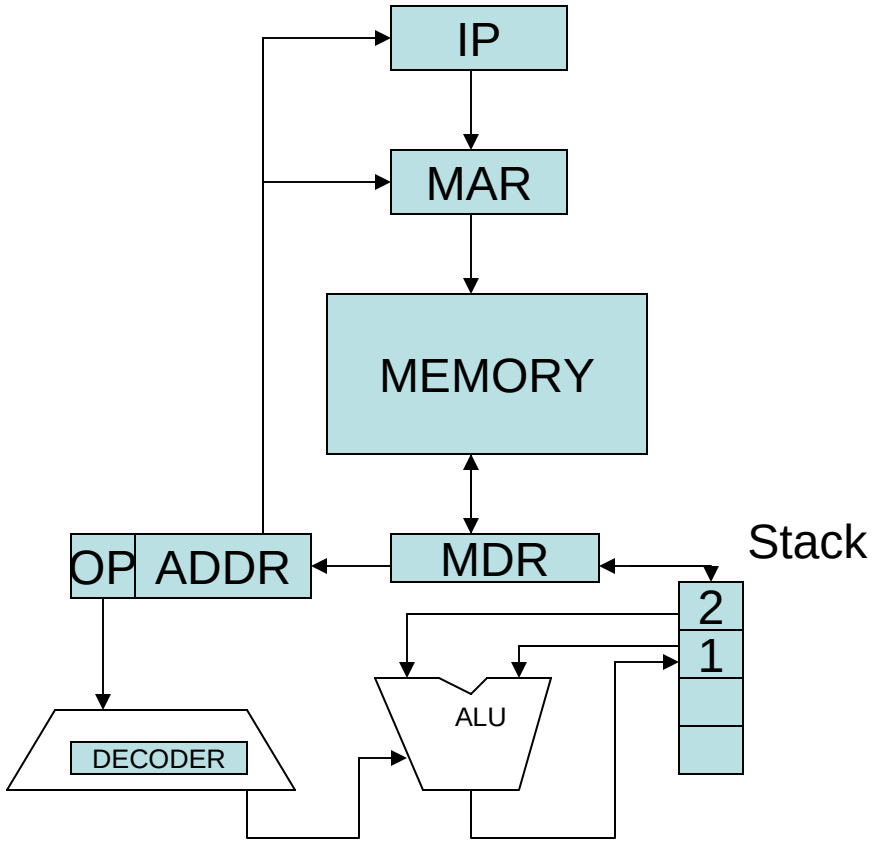
Stack Trace

- Loadi “1” 1 _ _ _
- Loadi “2”
- Add
- Store X



Cont'

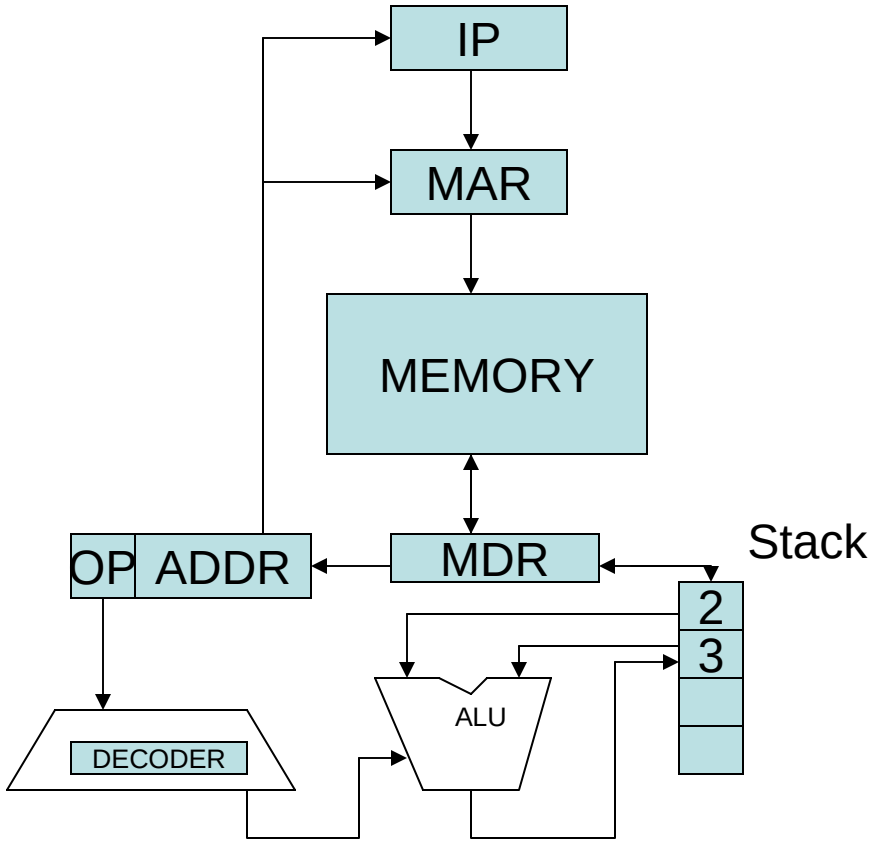
- Stack Trace
  - Loadi 1 1 _ _ _
  - Loadi 2 2 1 _ _
  - Add
  - Store X



ADD Step 1

Stack Trace

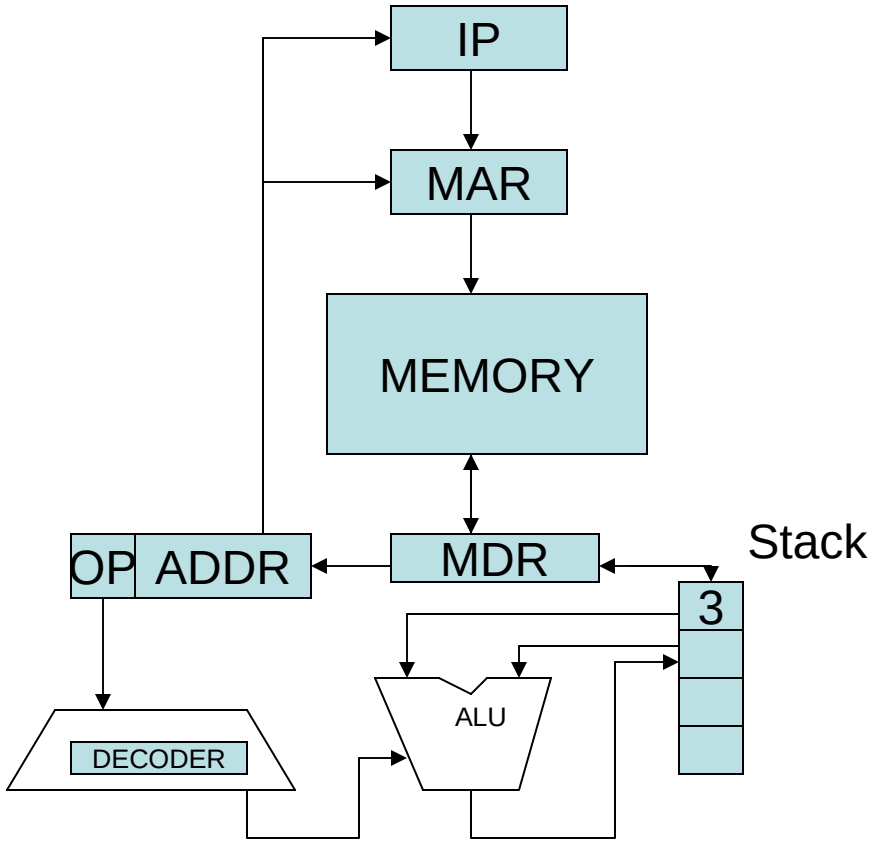
Push 1	1 _ _ _
Push 2	2 1 _ _
Add	2 3 _ _
Store X	



ADD step 2

Stack Trace

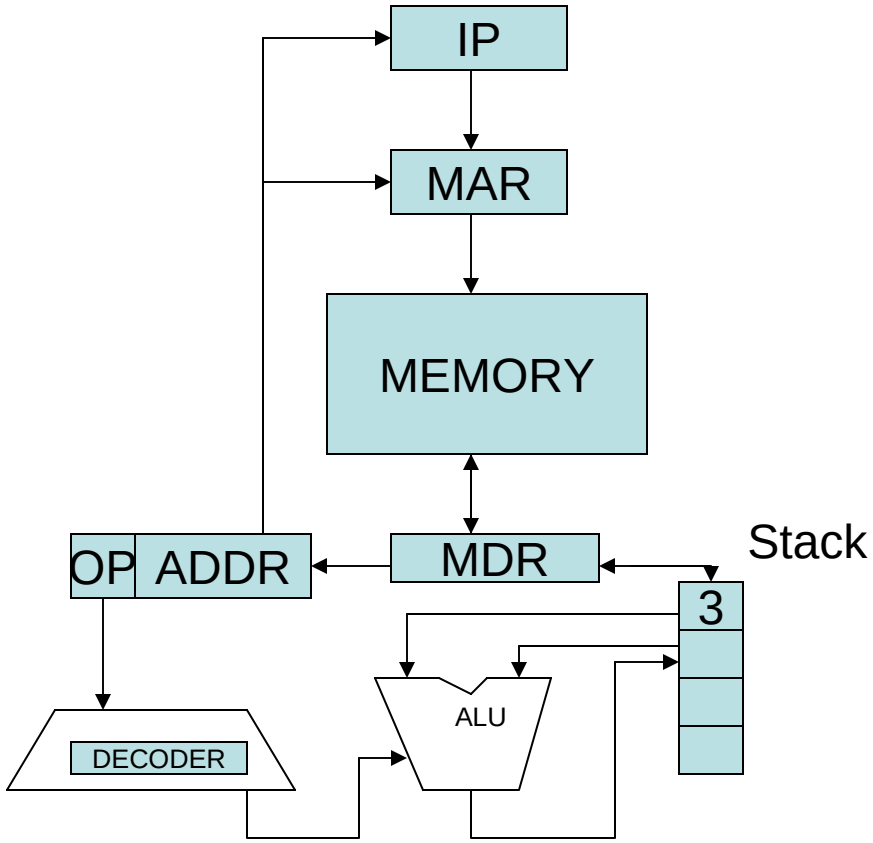
Push 1	1 _ _ _
Push 2	2 1 _ _
Add	3 _ _ _
Store X	



Before Store X is executed

Stack Trace

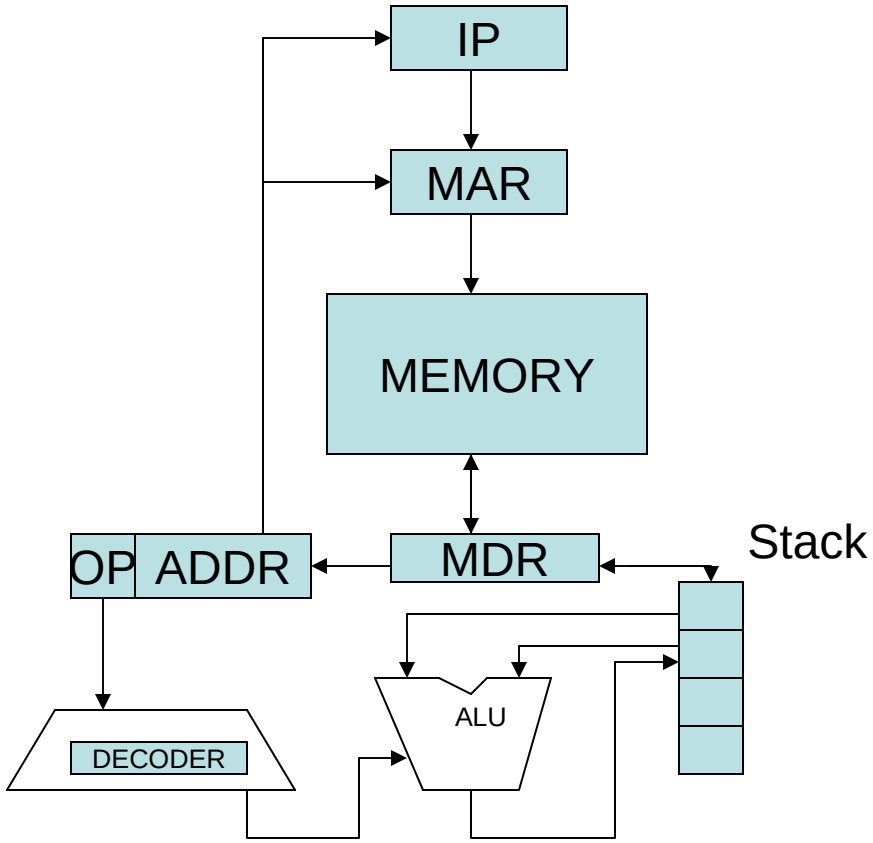
Push 1	1	_ _ _
Push 2	2	1 _ _
Add	3	_ _ _
Store X	3	_ _ _



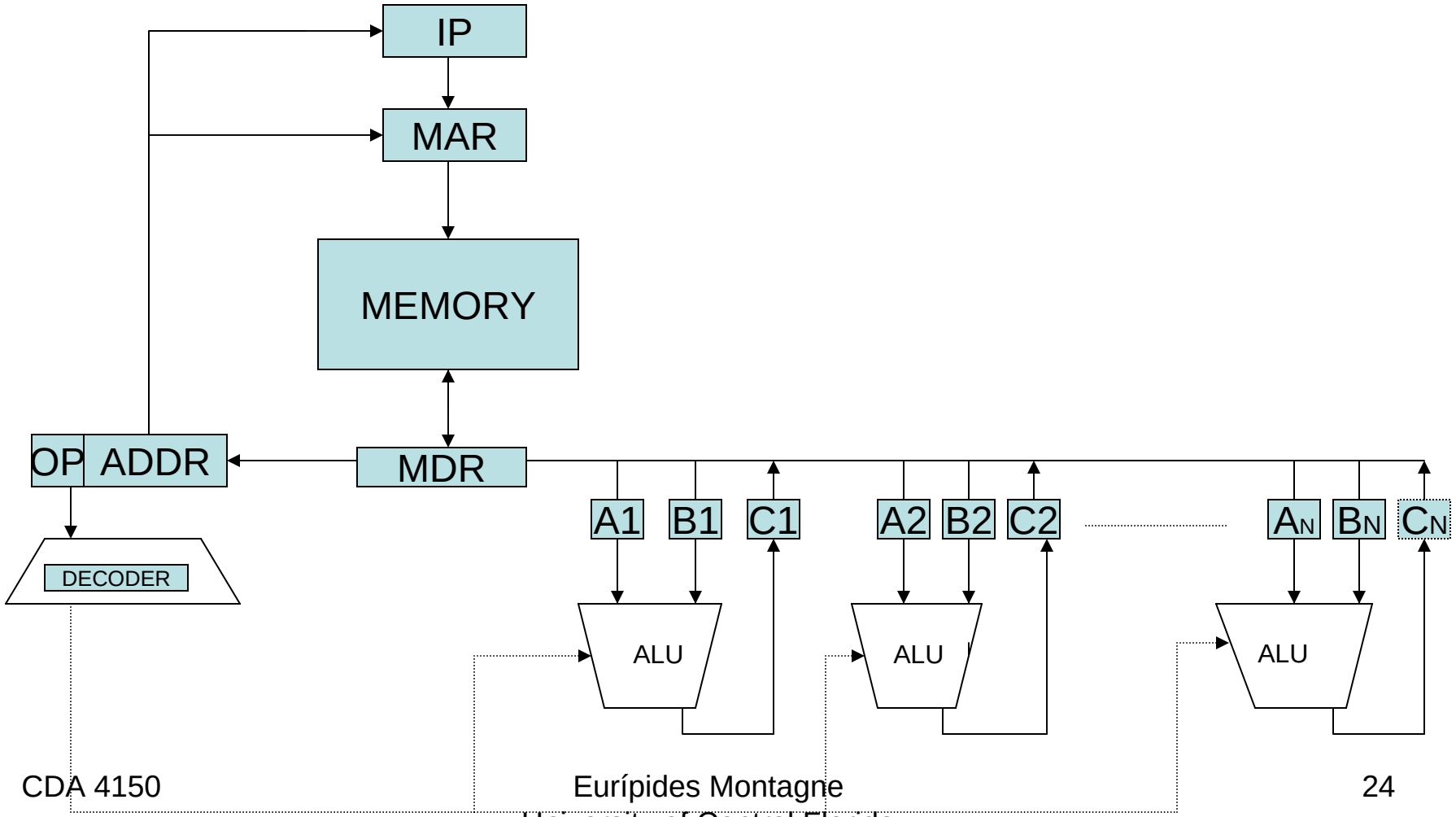
After Store X is executed

Stack Trace

Push 1	1 _ _ _
Push 2	2 1 _ _
Add	2 3 _ _
Store	_ _ _ _



SIMD(Array Processor)



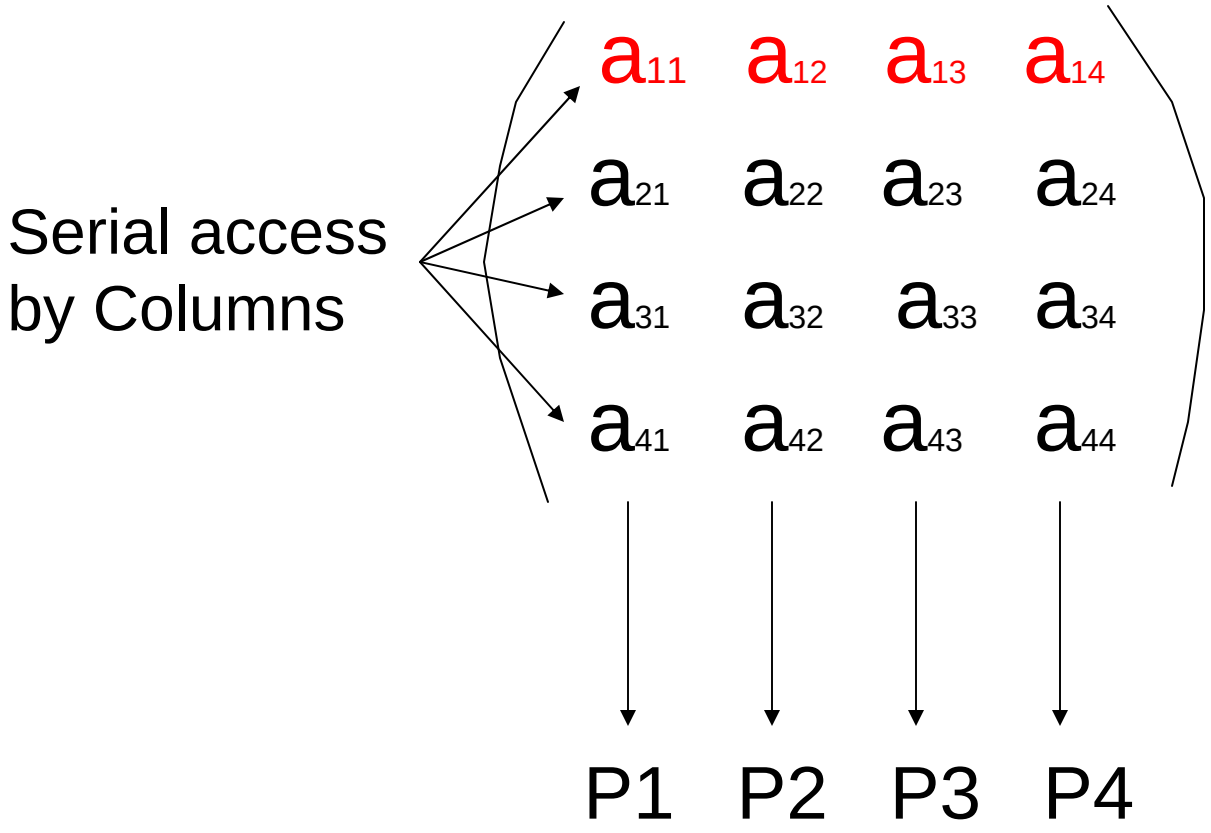
Array Processors

- One of the first Array Processors was the ILLIIAC IV
  - Load A1, V[1]
  - Load B1,Y[1]
  - Load A2, V[2]
  - Load B2, Y[2]
  - ……..
  - ……..
  - Load An, V[n]
  - Load Bn, Y[n]
  - ADD
  - Store C1, W[1]
  - Store C2, W[2]
  - Store C3, W[3]
  - ……..
  - ……..
  - Store Cn, W[n]

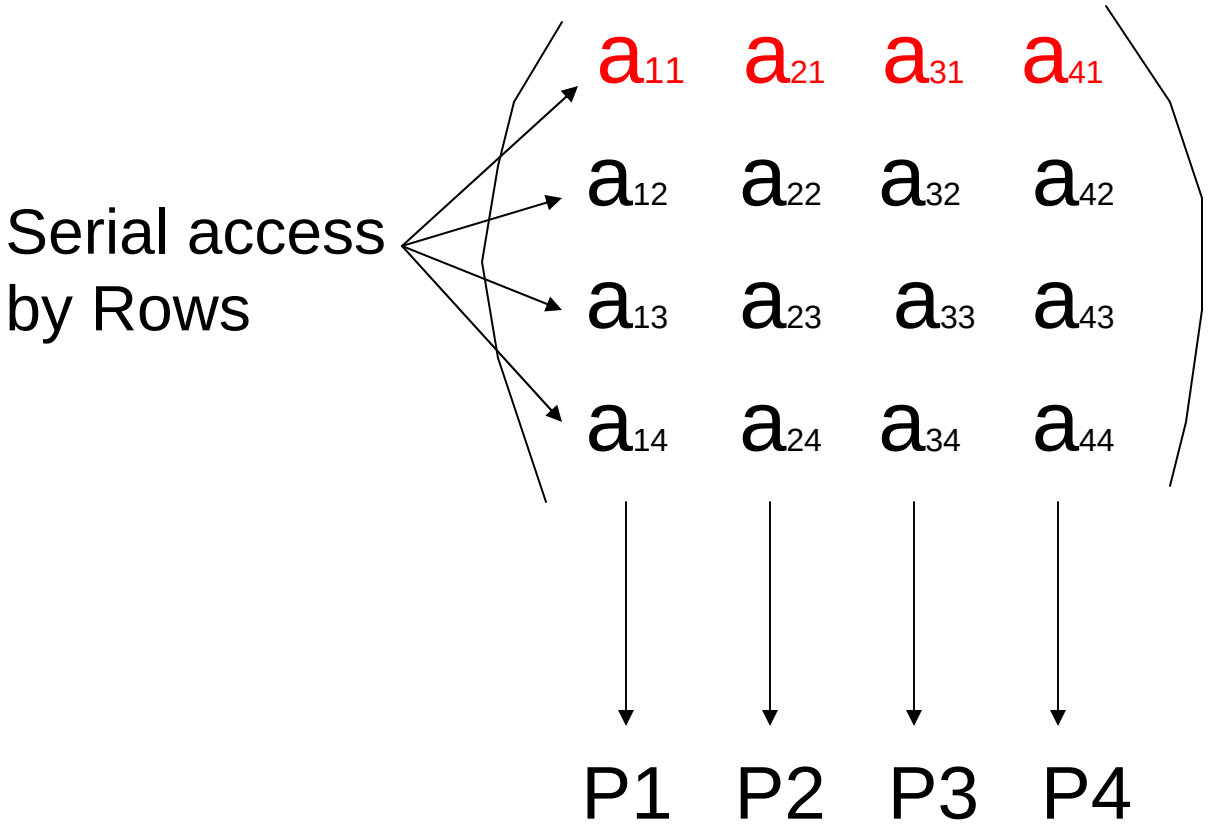
Matrix Access

- **Parallel access by Rows**
- **Parallel access by Columns**
- **Parallel access by Diagonals**
- **Skewed matrix representation**

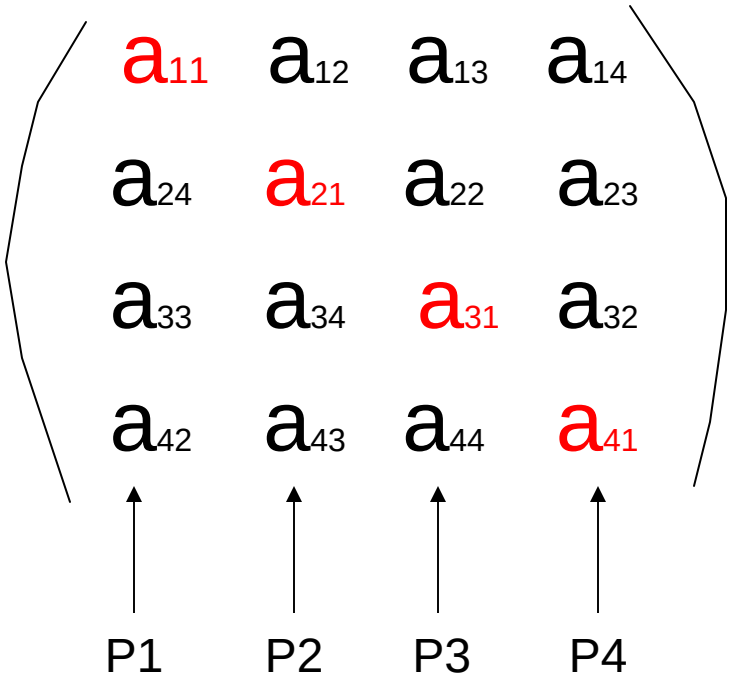
Parallel access by Row



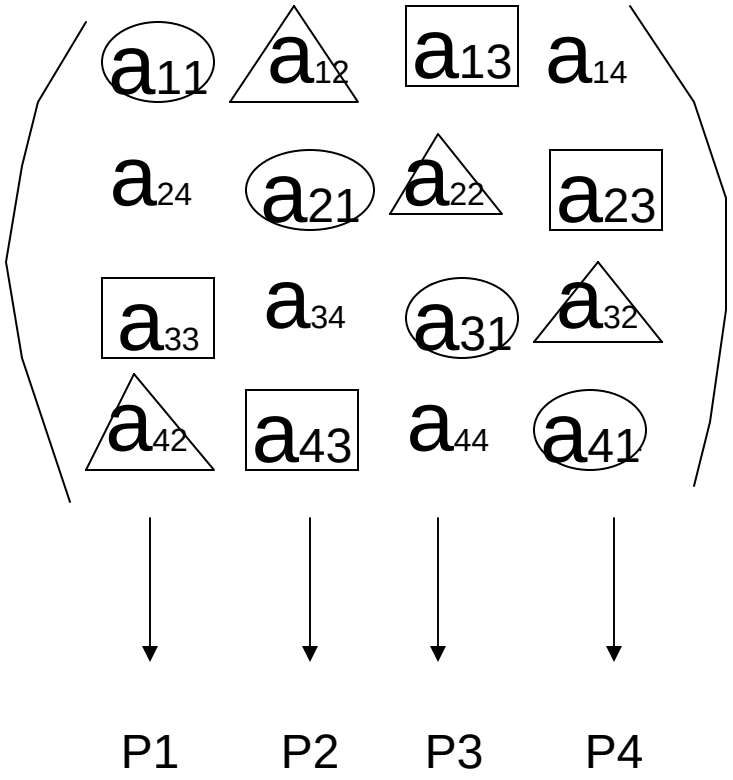
Parallel access by Column reordering is necessary



Parallel access by Diagonals



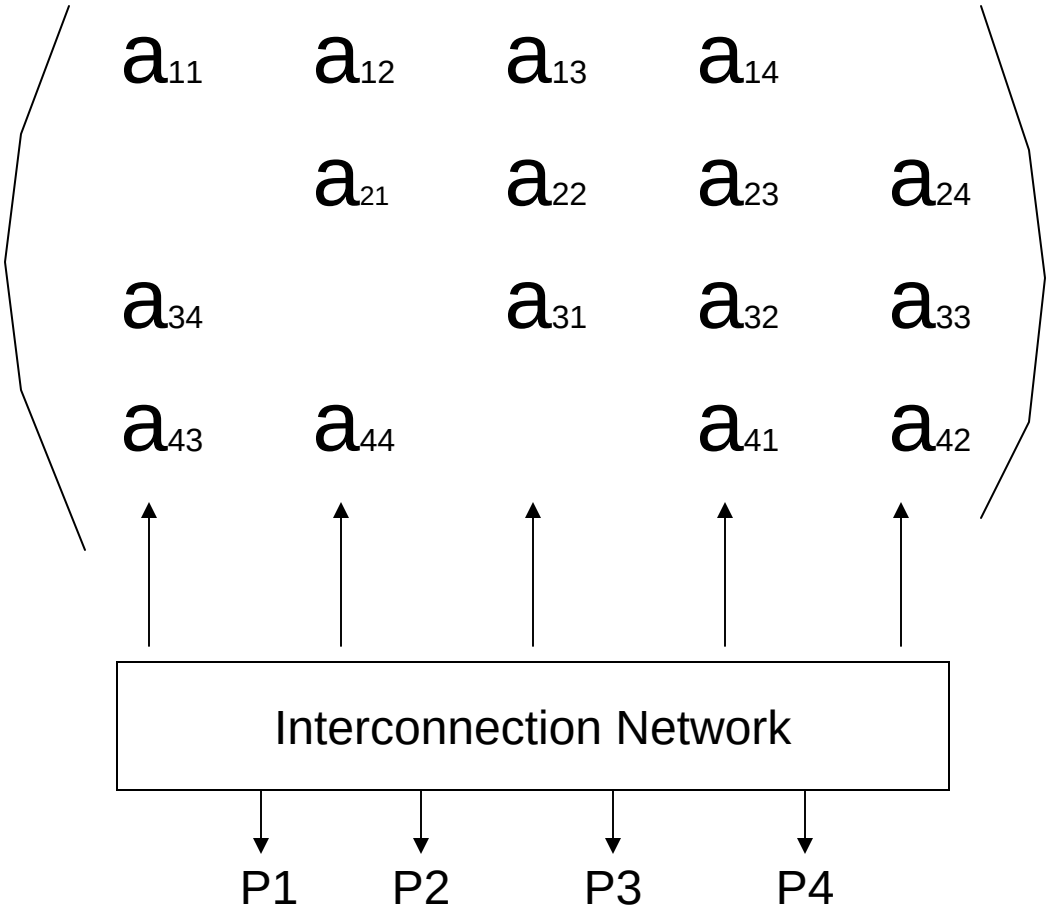
Parallel Column/Row Access



Skewed matrix representation

Parallel Column/Row/Diagonal Access

Skewed matrix representation (5 banks)



Pipelining

- Definition: Pipelining is an implementation technique whereby multiple instructions are overlapped in execution, taking advantage of parallelism that exists among actions needed to execute an instruction.
- Example: Pipelining is similar to an automobile assembly line.

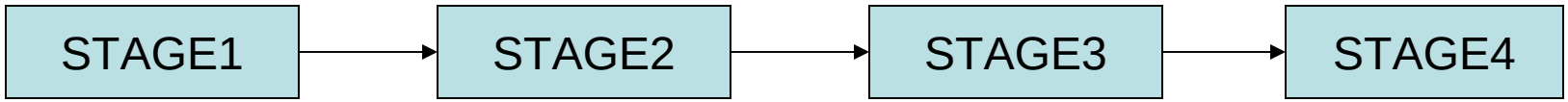
Pipelining: Automobile Assembly line

- T0: Frame|
- T1: Frame| wheels
- T2: Frame| wheels| Engine
- T3: Frame| Wheels| Engine| Body → New Car

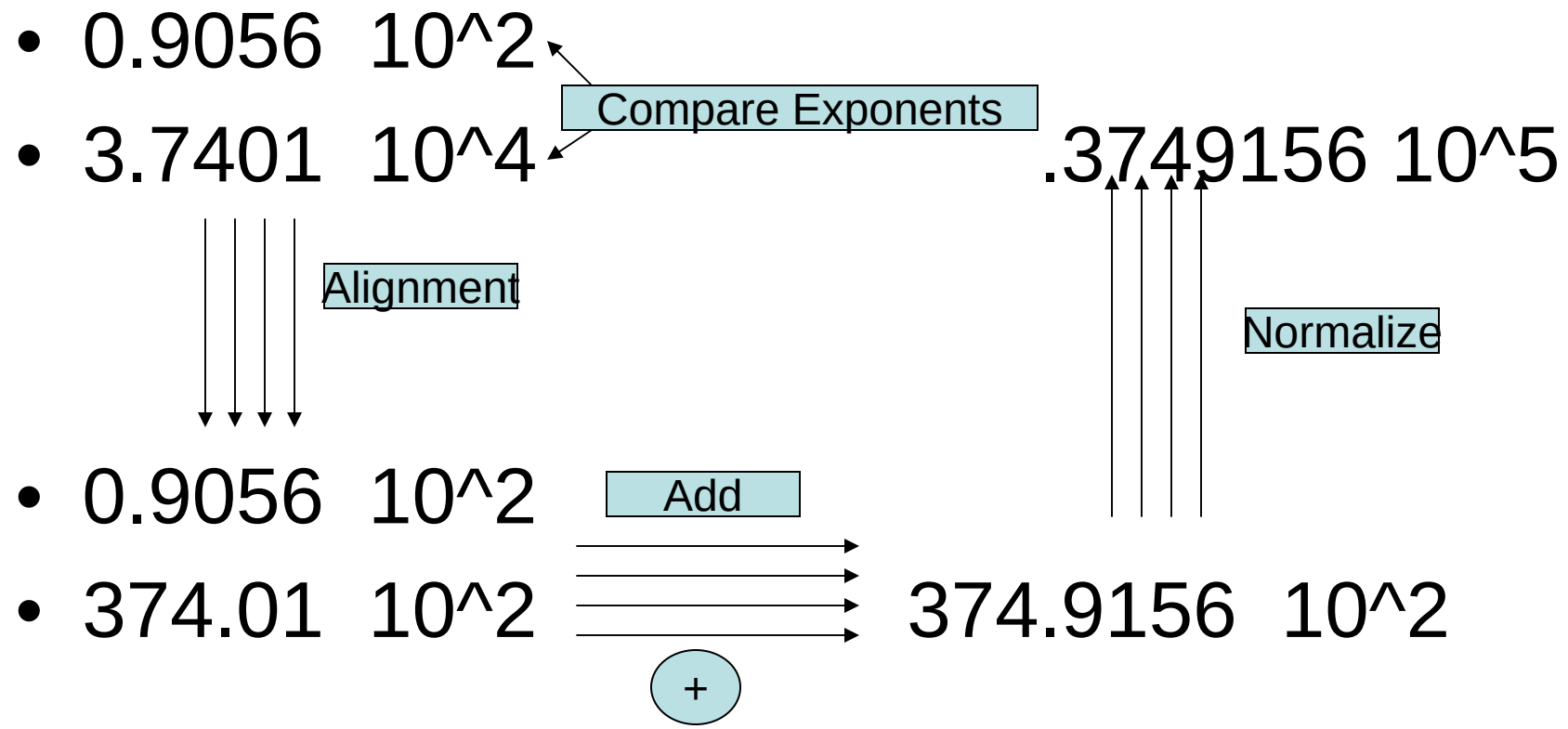
If it takes 1 hour to complete one car, and each of the above stages takes 15 minutes, then building the first car takes 1 hour; one car can produced every 15 minutes. This same principle can be applied to computer instructions.

Pipelining: Floating point addition

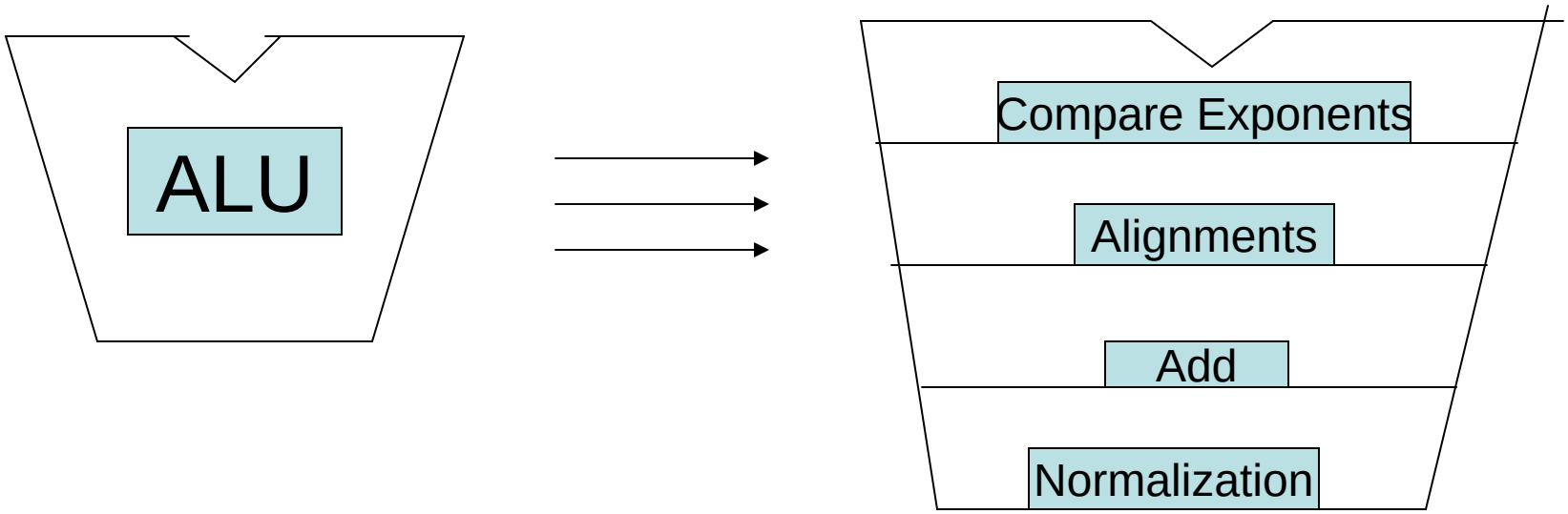
- Suppose a floating point addition operation could be divided into 4 stages, each completion ¼ of the total addition operation.
- Then the following chart would be possible.



Example


0.9056 10^2
3.7401 10^4
Compare Exponents
.3749156 10^5
Alignment
Normalize
0.9056 10^2
Add
374.01 10^2
374.9156 10^2
+

Floating point unit



The steps

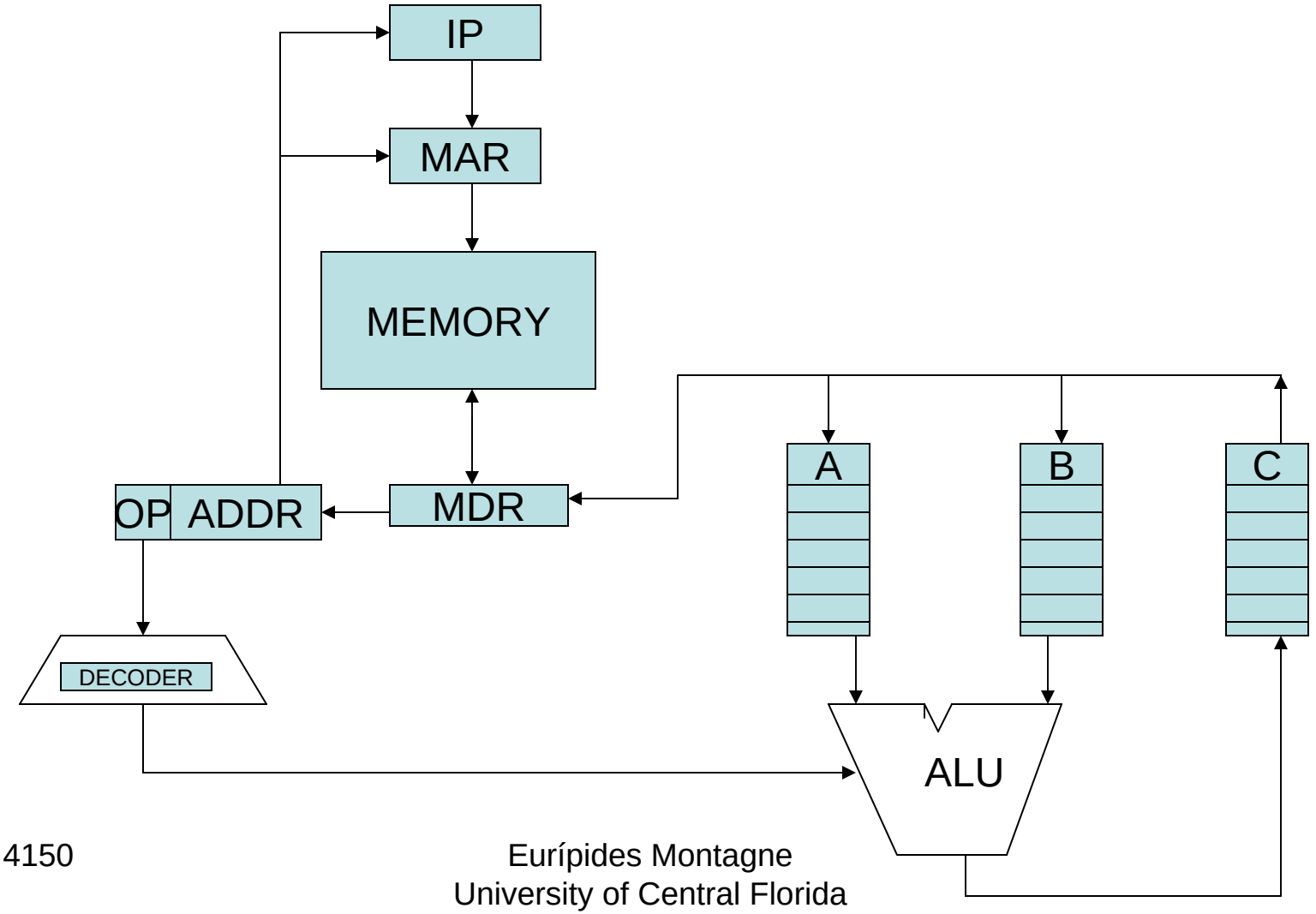
- Step one: Compare and choose the exponents.
- Step two: Set both numbers to the same exponent.
- Step three: Perform addition/subtraction on the two numbers.
- Last step: Normalization.

Vector processors

Vector processor Characteristics:

- Pipelining is used in processing.
- Vector Registers are used to provide the ALU with constant input.
- Memory interleaving is used to load input to the vector registers.
- AKA Supercomputers.
- the CRAY-1 is regarded as the first of these types.

Vector Processors: Diagram



Vector Processing: Compilers

- The addition of vector processing has led to vectorization in compiler design.

Example: the following loop construct:

FOR I, 1 to N

C[i] ← A[i]+ B[i]

Can be unrolled into the following instruction:

C[1] ← A[1]+B[1]

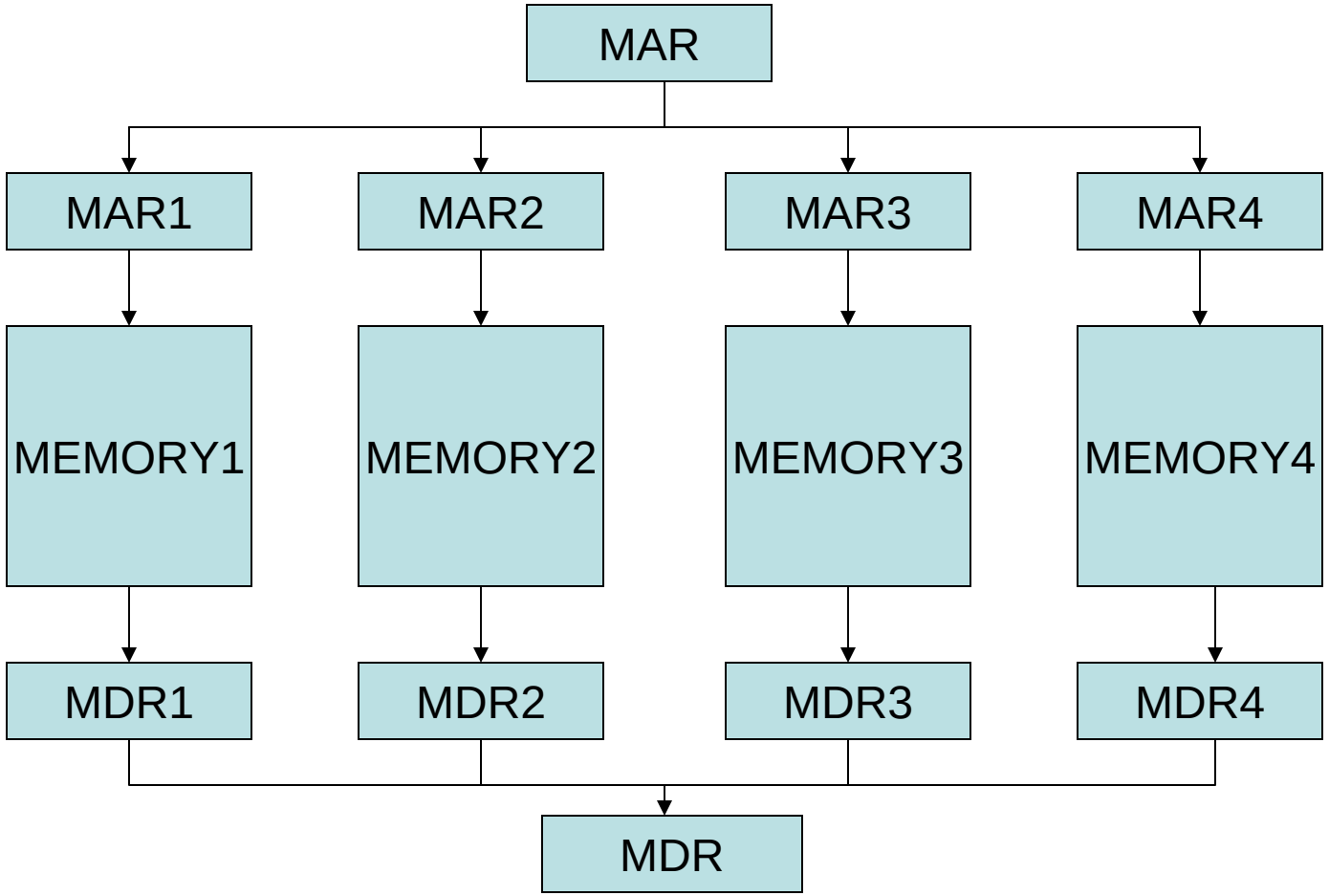
C[2] ← A[2]+B[2]

C[3] ← A[3]+B[3]…..

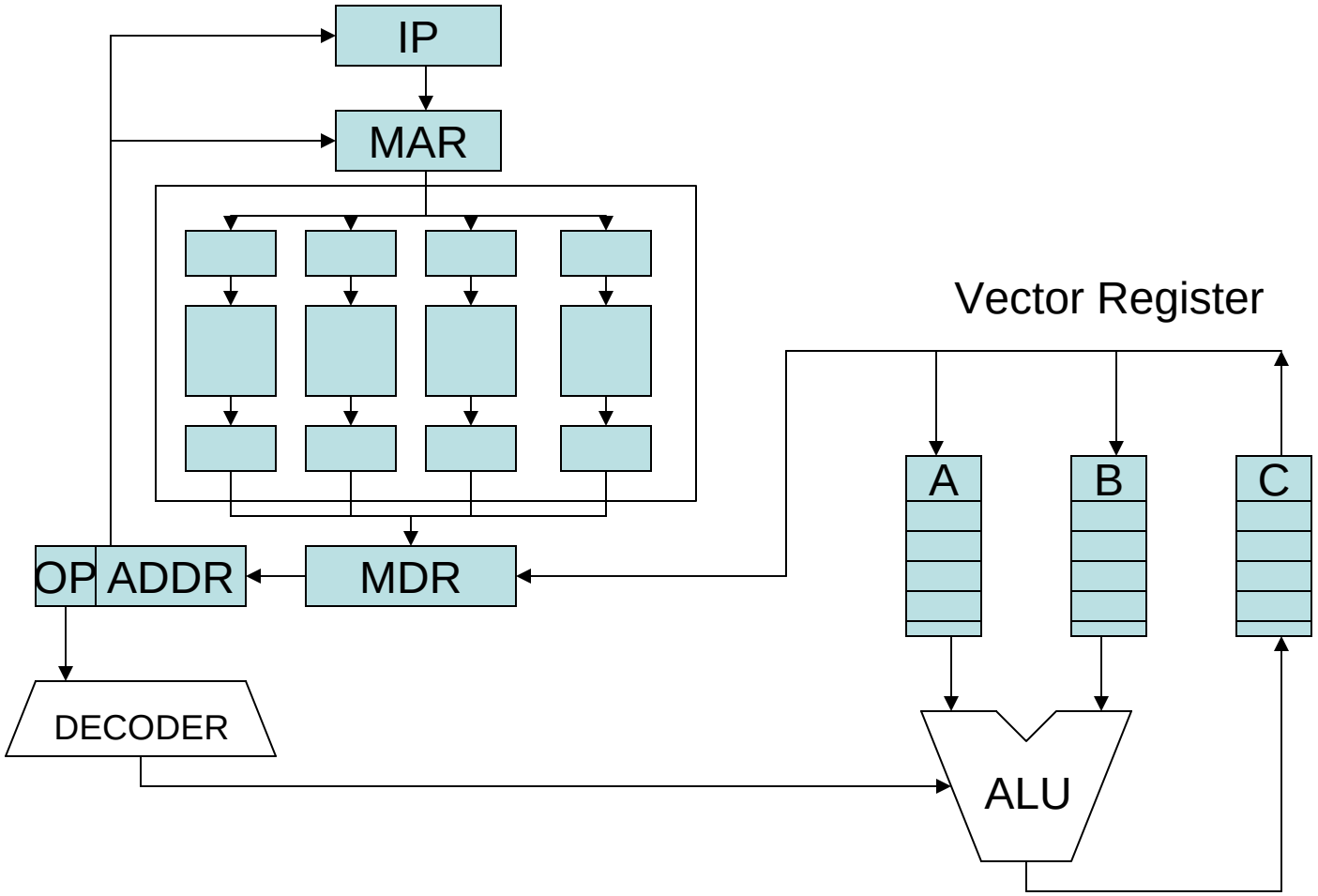
Memory Interleaving

- Definition: Memory Interleaving is a design used to gain faster access to memory, by organizing memory into separate memory banks, each with their own MAR (memory address register). This allows parallel access and eliminates the required wait for a single MAR to finish a memory access.

Memory Interleaving: Diagram



Vector Processors & Memory Interleaving Diagram



Multiprocessor Machines (MIMD)