Systolic Arrays and Data Flow

3/22/04

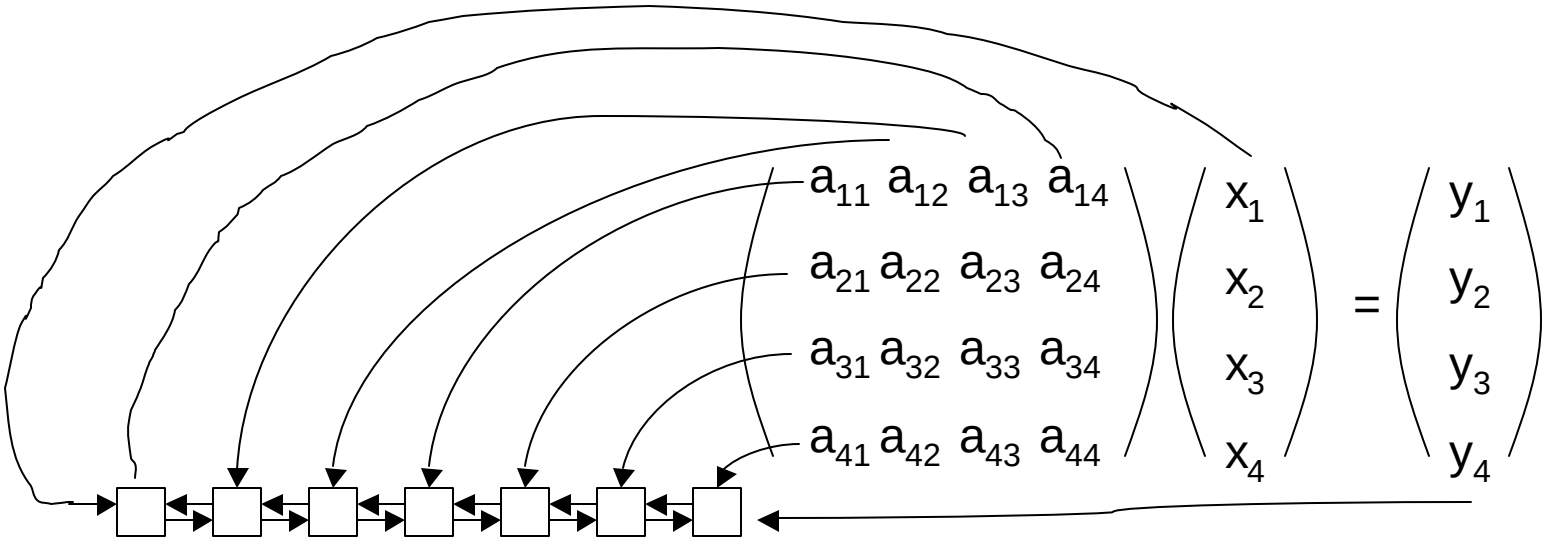
Doug Hathaway

Justin Griffin

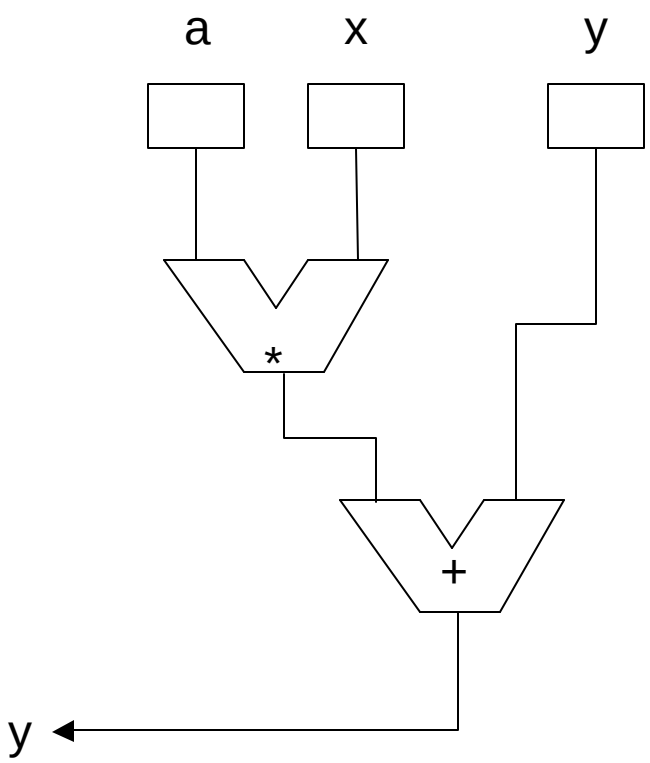
Systolic Arrays

Multiplication of (a * x)

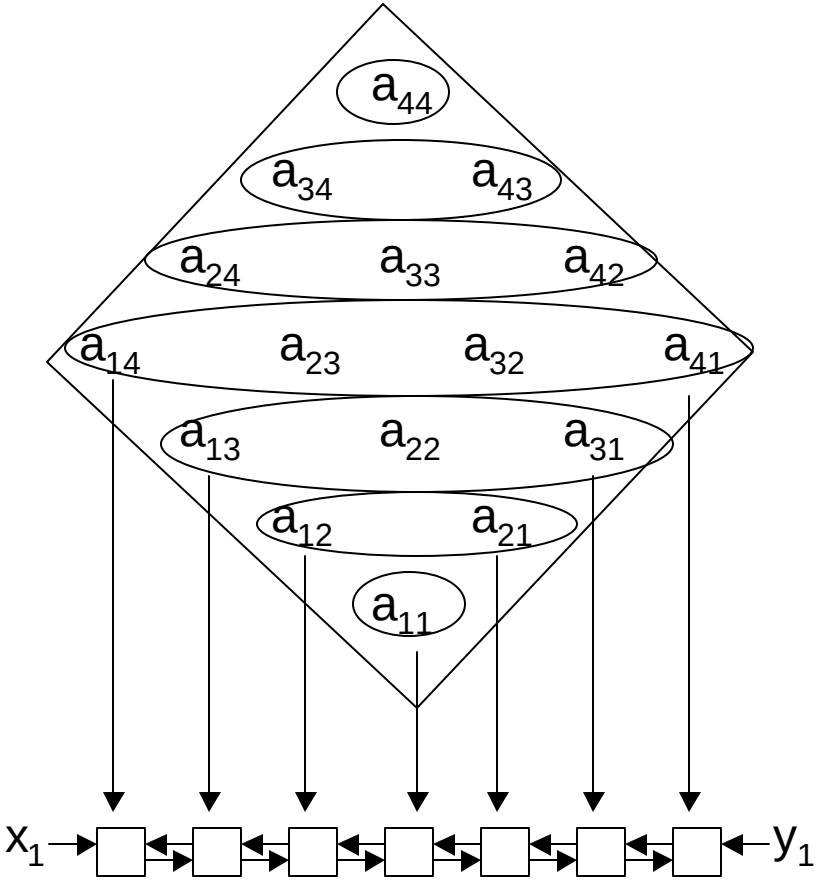
row * column



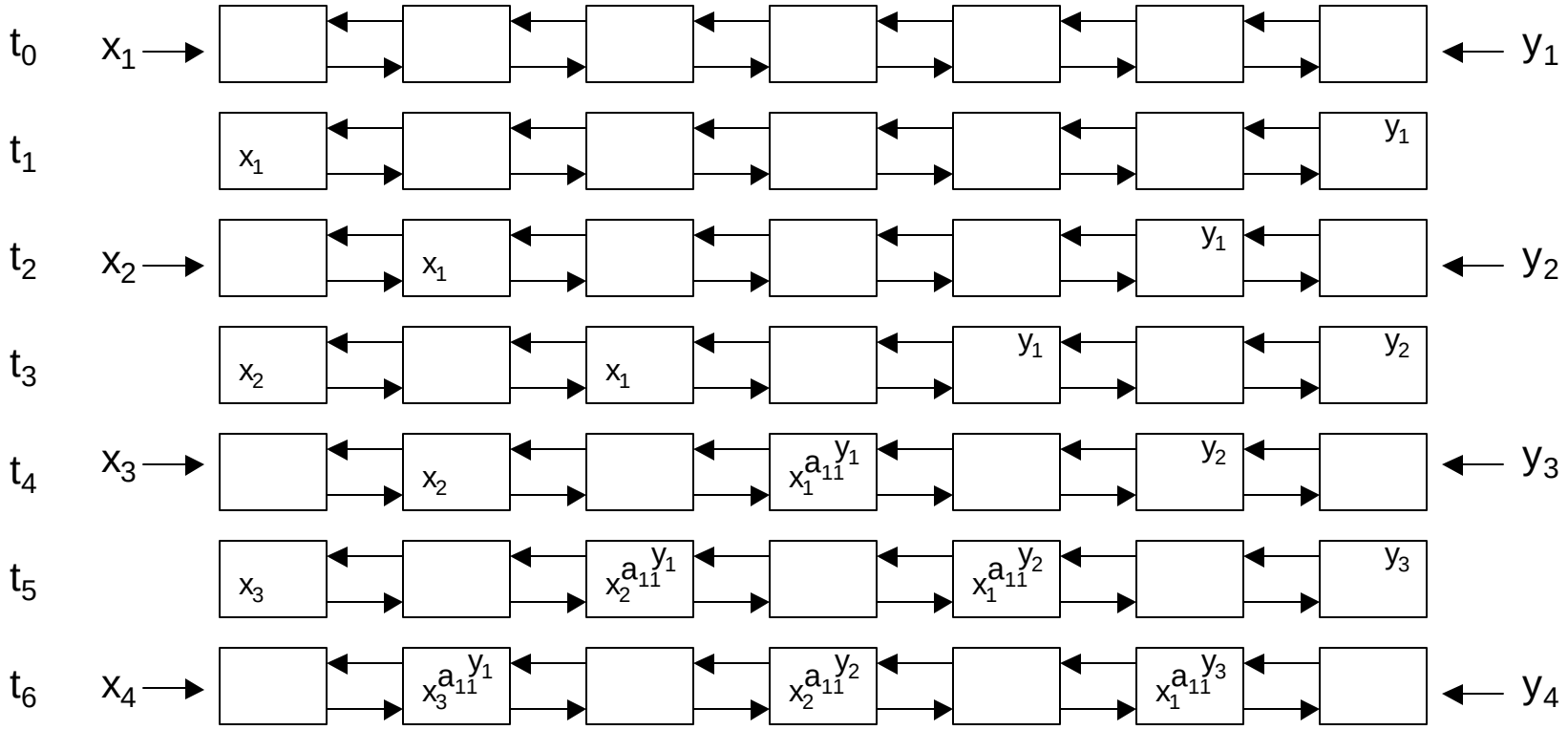
Architecture



Systolic Array



Timing Diagram for Systolic Arrays



Y results

- $Y_1 = a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4$
- $Y_2 = a_{21}x_1 + a_{22}x_2 + a_{23}x_3 + a_{24}x_4$
- $Y_3 = a_{31}x_1 + a_{32}x_2 + a_{33}x_3 + a_{34}x_4$

Data Flow

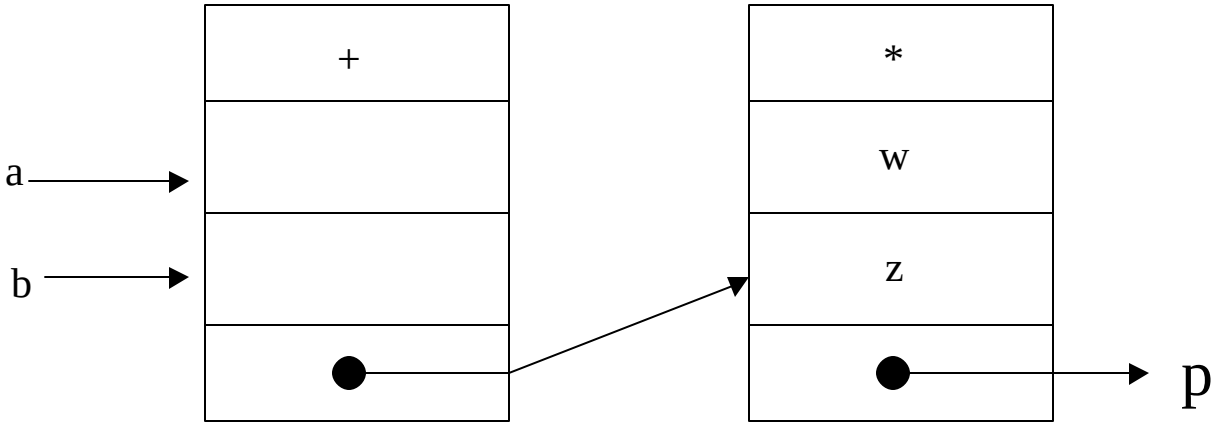
Instruction Template

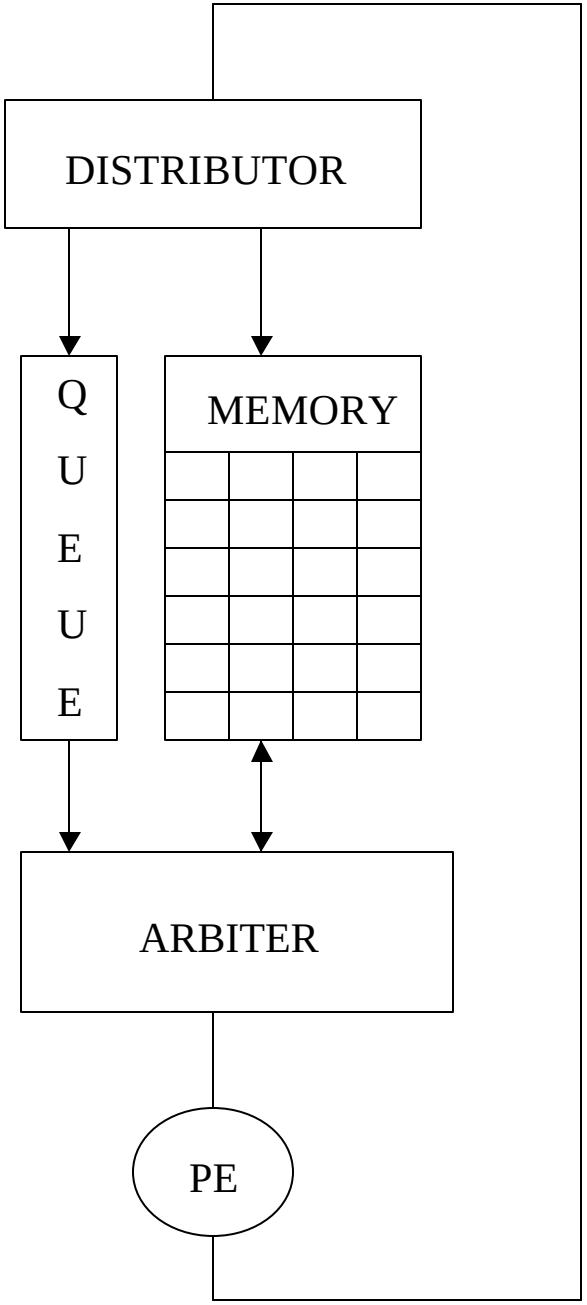
OPCODE
VALUE
VALUE
ADDRESS

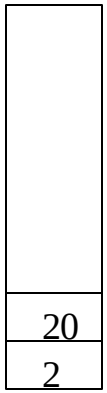
(RESULT)

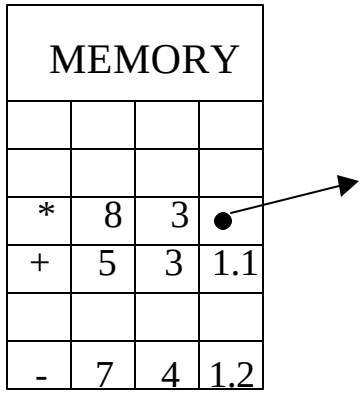
z ß a + b

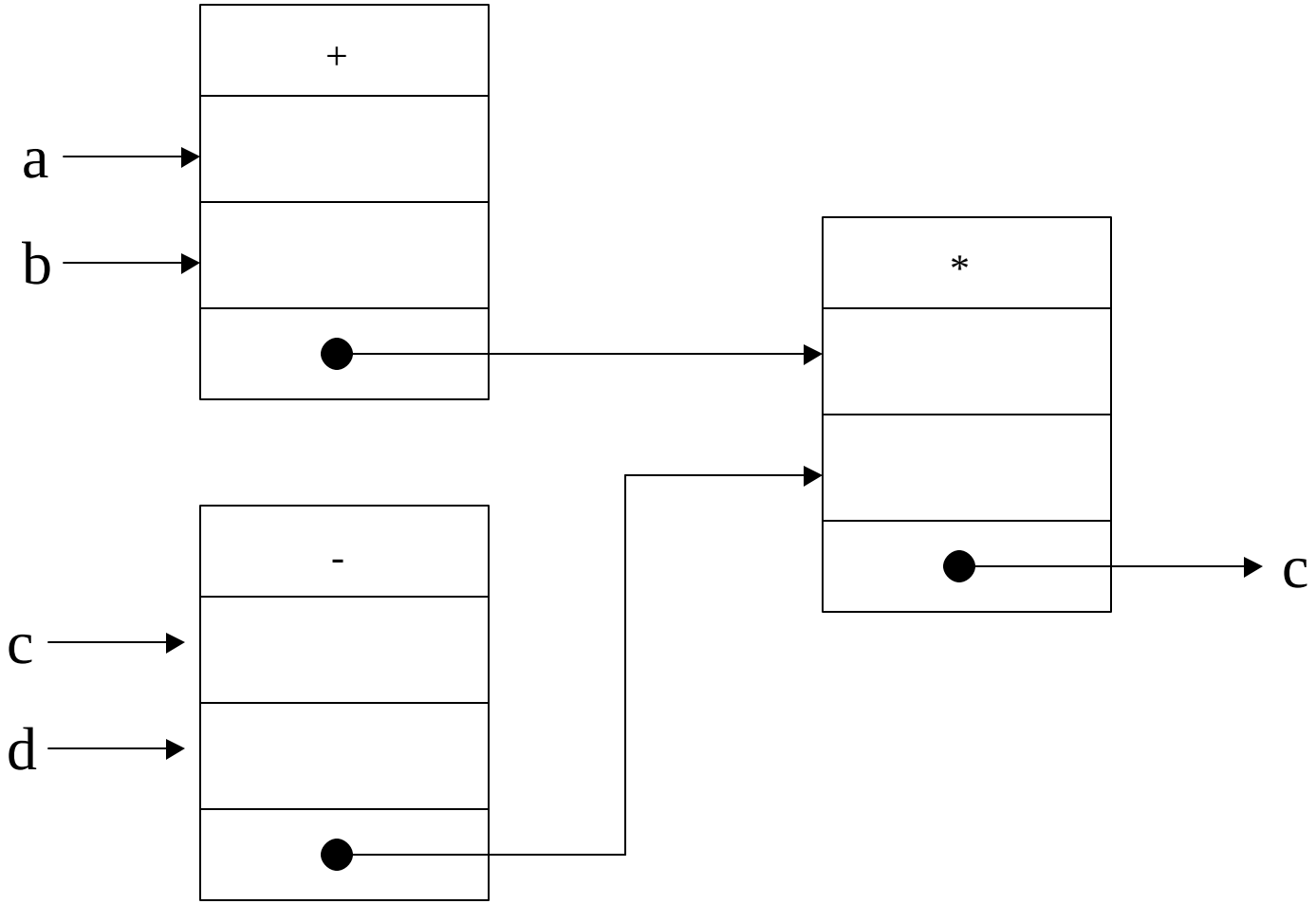
p ß z * w




DISTRIBUTOR
Q
U
E
U
E
MEMORY
ARBITER
PE


20
2


MEMORY
*
8
3
+
5
3
1.1
-
7
4
1.2

Another example

C ß (a + b) * (c – d)