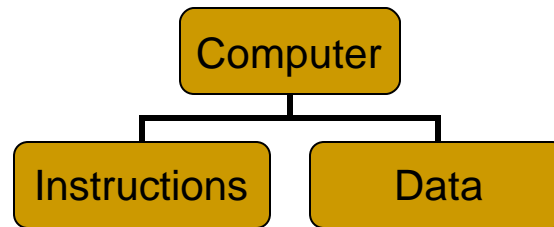

Flynn's Taxonomy

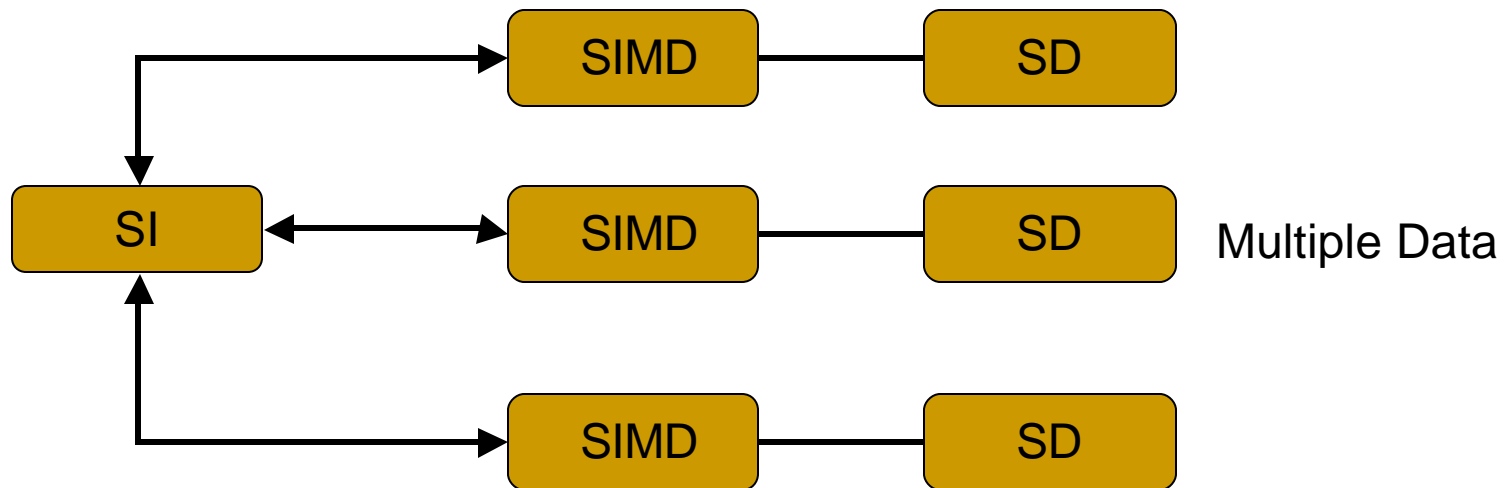
- Michael Flynn (from Stanford)
 - Made a characterization of computer systems which became known as Flynn's Taxonomy



SISD – Single Instruction Single Data Systems



SIMD – Single Instruction Multiple Data Systems “Vector Processors”

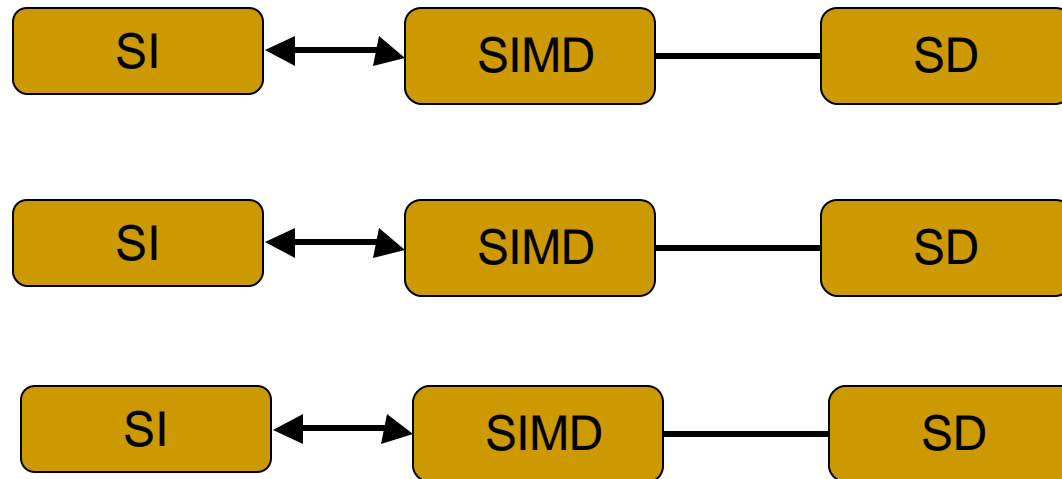


MIMD Multiple Instructions Multiple Data Systems

“Multi Processors”

Multiple Instructions

Multiple Data

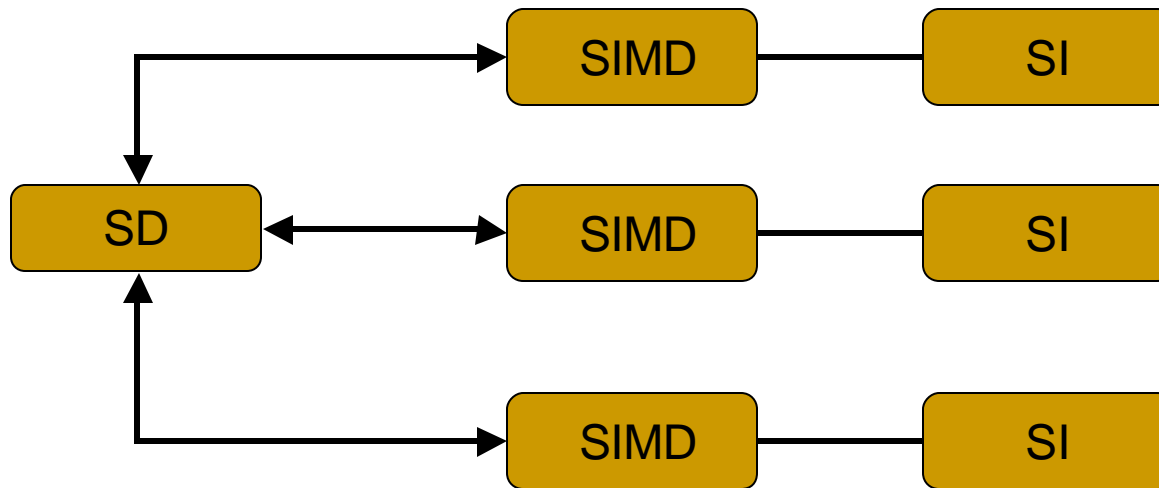


MISD – Multiple Instructions / Single Data Systems

- Some people say “pipelining” lies here, but this is debatable

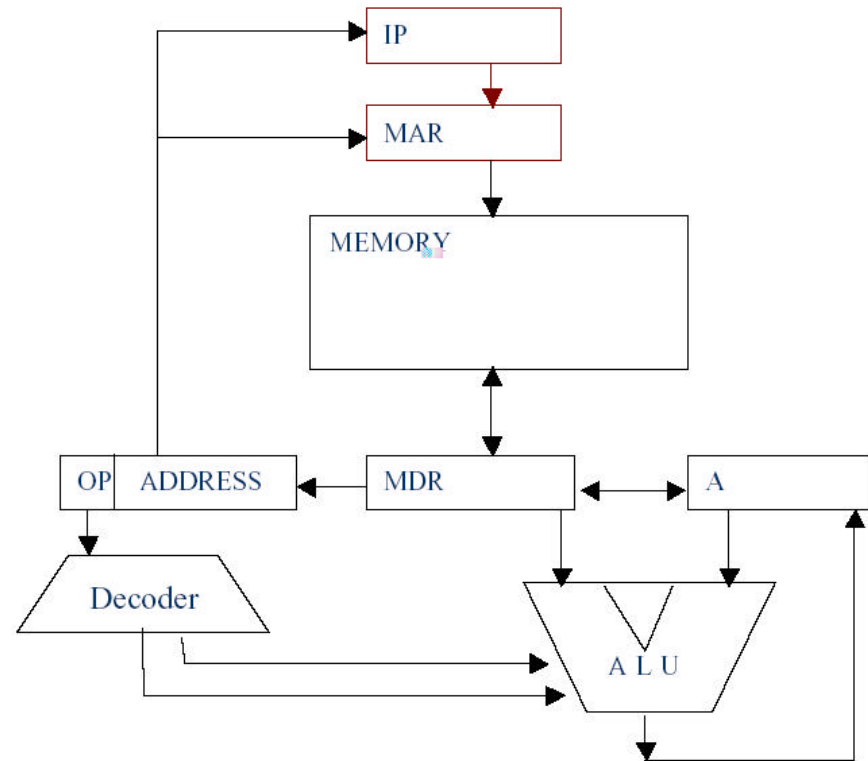
Single Data

Multiple Instructions



Abbreviations

- PC – Program Counter
- MAR – Memory Access Register
- M – Memory
- MDR – Memory Data Register
- A – Accumulator
- ALU – Arithmetic Logic Unit
- IR – Instruction Register
- OP – Opcode
- ADDR – Address
- CLU – Control Logic Unit



LOAD X

- $MAR \leftarrow PC$
 - $MDR \leftarrow M[MAR]$
 - $IR \leftarrow MDR$
 - $MAR \leftarrow IR[ADDR]$
 - $DECODER \leftarrow IR[OP]$
 - $MDR \leftarrow M[MAR]$
 - $A \leftarrow MDR$
-

ADD

- $MAR \leftarrow PC$
 - $MDR \leftarrow M[MAR]$
 - $IR \leftarrow MDR$
 - $MAR \leftarrow IR[ADDR]$
 - $DECODER \leftarrow IR[OP]$
 - $MDR \leftarrow M[MAR]$
 - $A \leftarrow A + MDR$
-

STORE

- $MDR \leftarrow A$
- $M[MAR] \leftarrow MDR$

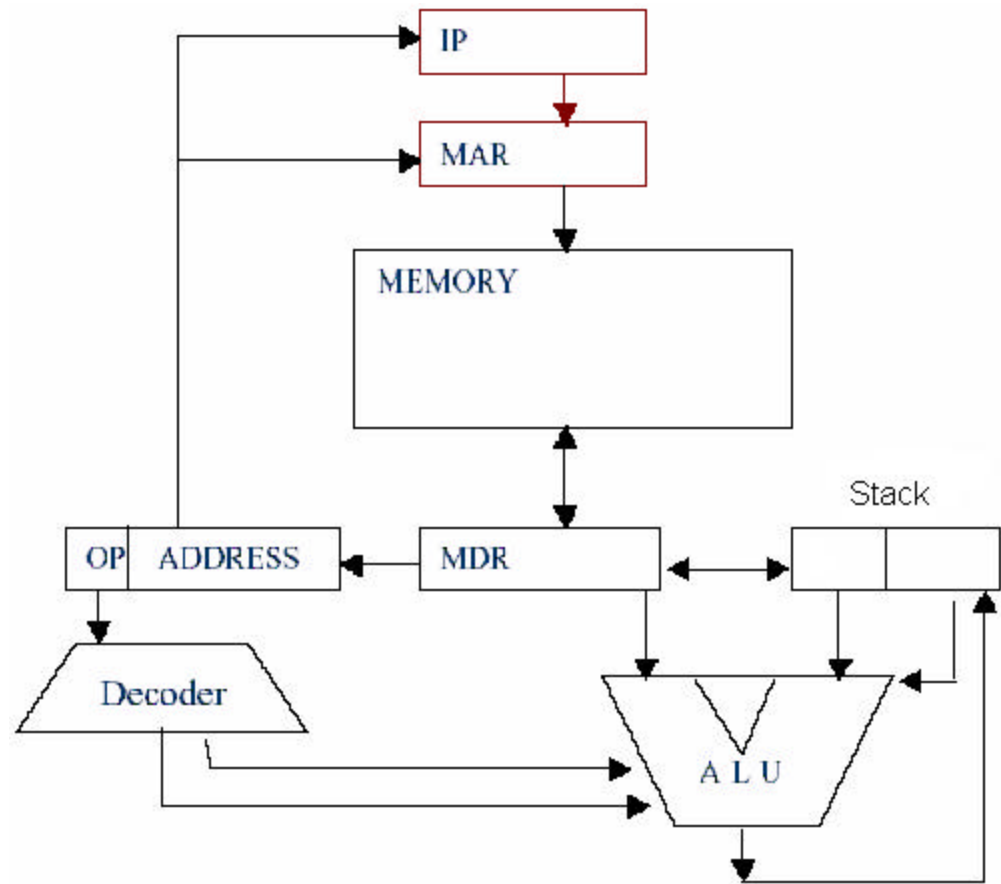
SISD Stack Machine

- Stack Trace

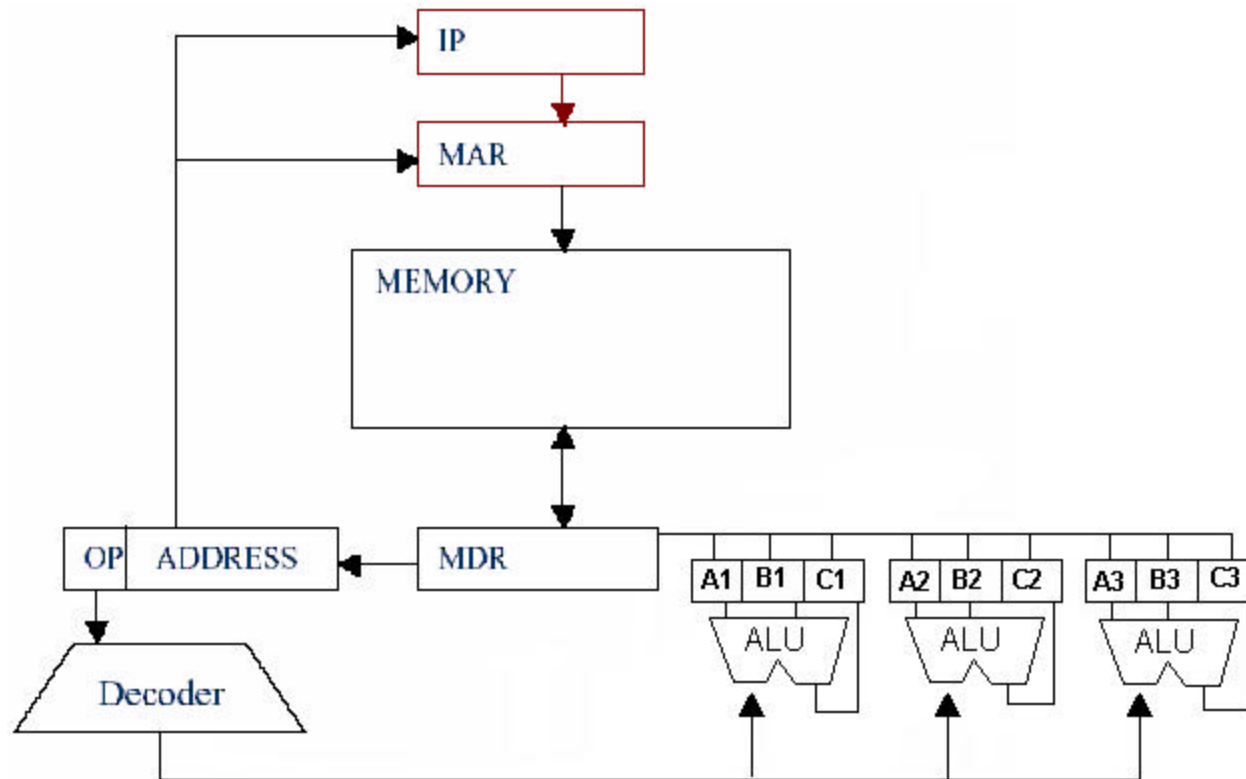
- Push 1 1 _
- Push 2 2 1
- Add 2 3
- Pop _ 3
- Pop C _ _

- First Stack Machine

- B5000



Array Processor



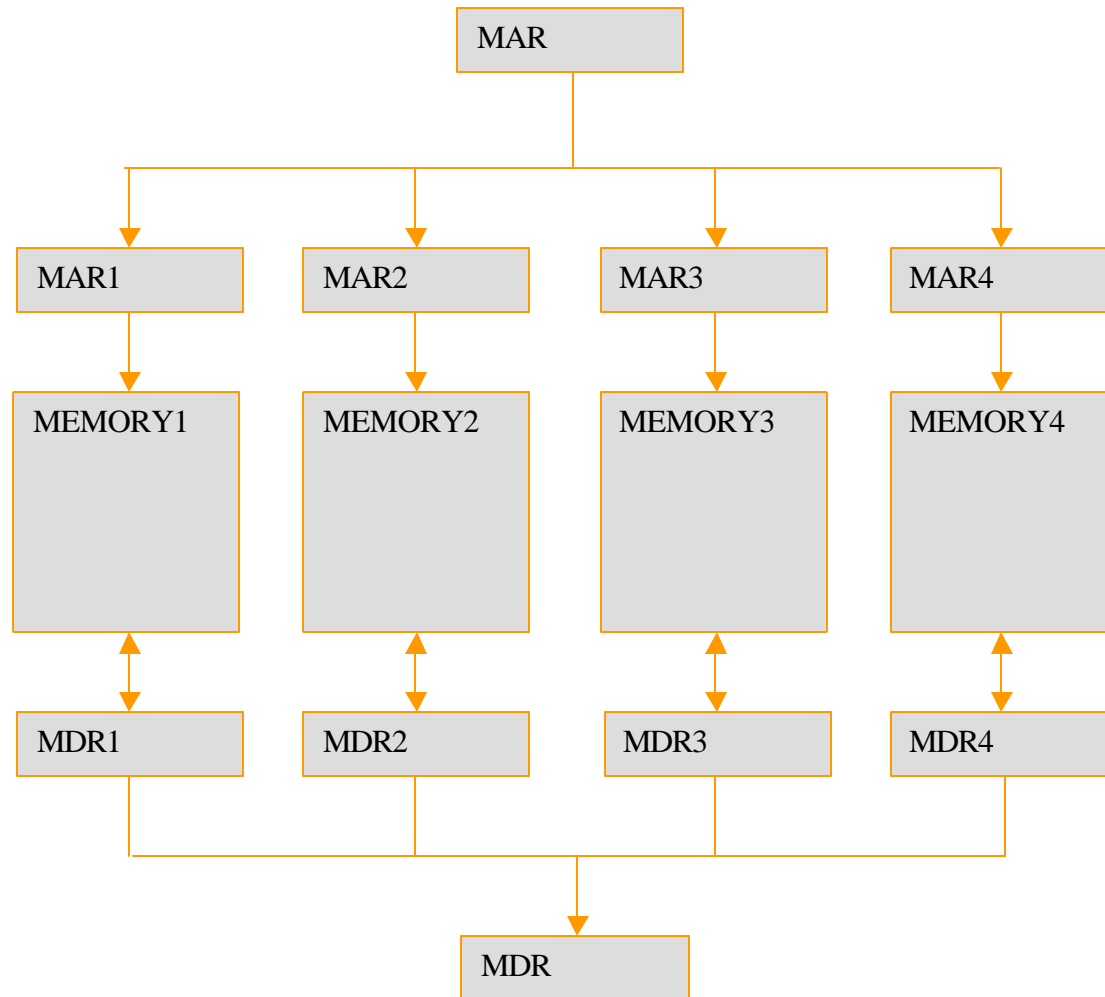
Array Processors

- One of the first Array Processors was the ILLIAC IV
 - Load A1, V[1]
 - Load B1, Y[1]
 - Load A2, V[2]
 - Load B2, Y[2]
 - Load A3, V[3]
 - Load B3, Y[3]
 - ADDALL
 - Store C1, W[1]
 - Store C2, W[2]
 - Store C3, W[3]
-

Memory Interleaving

Definition: Memory interleaving is a design used to gain faster access to memory, by organizing memory into separate memories, each with their own MAR (memory address register). This allows parallel access and eliminates the required wait for a single MAR to finish a memory access.

Memory Interleaving: Diagram



Pipelining

Definition: Pipelining is an implementation technique whereby multiple instructions are overlapped in execution, taking advantage of parallelism that exists among actions needed to execute an instruction.

Example: Pipelining is similar to an automobile assembly line.

Pipelining: Automobile Assembly Line

T_0 : Frame |

T_1 : Frame | Wheels

T_2 : Frame | Wheels | Engine

T_3 : Frame | Wheels | Engine | Body.

If it takes 1 hour to complete one car, and each of the above stages takes 15 minutes, then one car can be produced every 15 minutes. This same principle can be applied to computer instructions.

Pipelining: Floating point addition

Suppose a floating point addition operation could be divided into 4 stages, each completing $\frac{1}{4}$ of the total addition operation. Then the following chart would be possible.



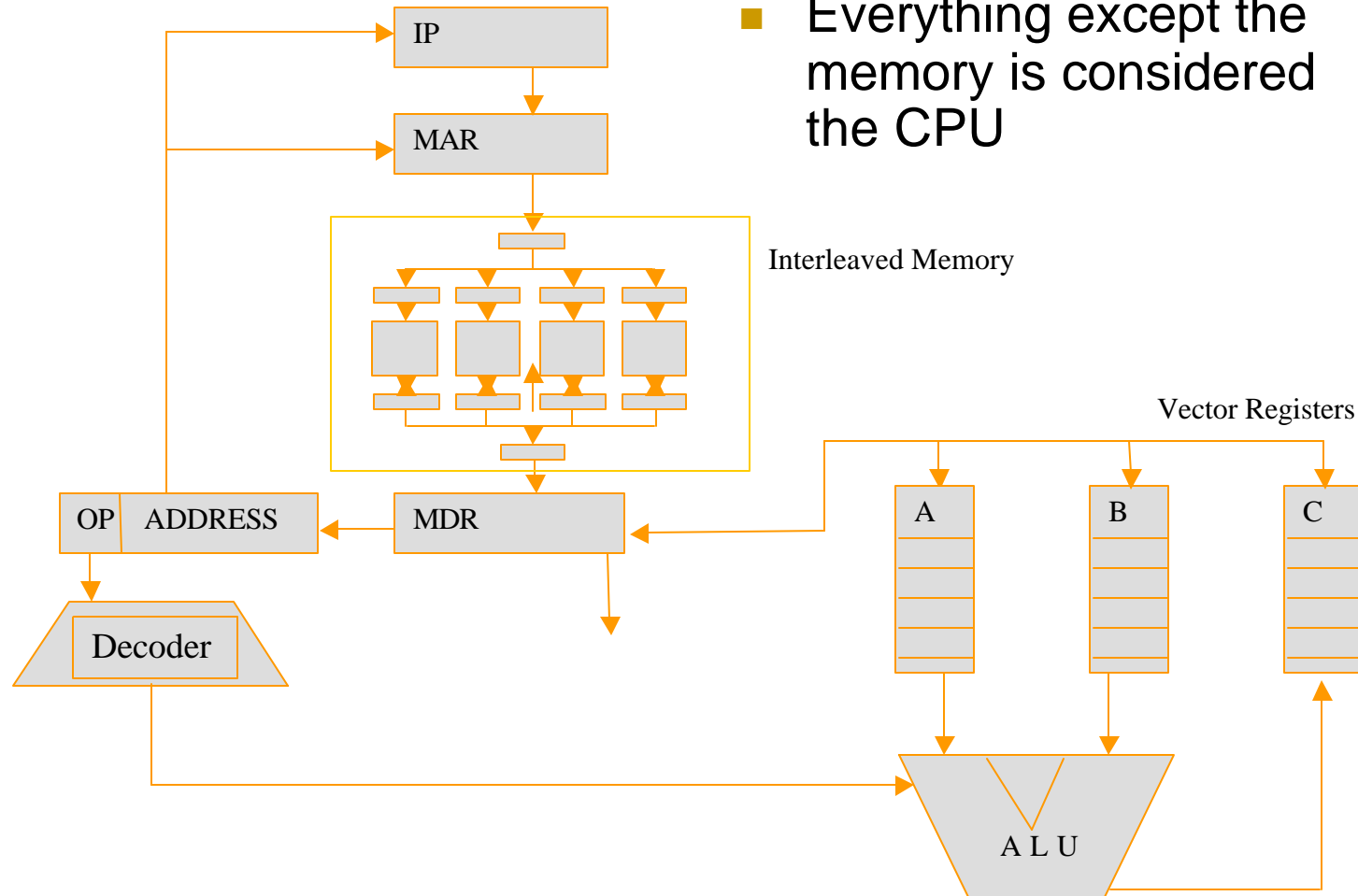
Vector Processors

Vector Processor Characteristics:

- Pipelining is used in processing.
 - Vector Registers are used to provide the ALU with constant input.
 - Memory interleaving is used to load input to the Vector registers.
 - AKA Supercomputers.
 - The CRAY-1 is regarded as the first of these types.
-

Vector Processors: Diagram

- Everything except the memory is considered the CPU



Vector Processing: Compilers

- The addition of vector processing has led to vectorization in compiler design.

Example: The following loop construct:

FOR I, 1 to N

$C[i] \leftarrow A[i] + B[i]$

Can be divided into the following instructions:

$C[1] \leftarrow A[1] + B[1]$

$C[2] \leftarrow A[2] + B[2]$

$C[3] \leftarrow A[3] + B[3] \dots$

Multiprocessor Machines (MIMD)

